SYLLABUS

1. Data about the program of study

1.1 Institution	Technical University of Cluj-Napoca
1.2 Faculty	Electronics, Telecommunications and Information Technology
1.3 Department	Bases of Electronics
1.4 Field of study	Electronic Engineering, Telecommunications and Information Technologies
1.5 Cycle of study	Master of of Science
1.6 Program of study/Qualification	Integrated Circuits and Systems / Engineer
1.7 Form of education	Full time
1.8 Subject code	

2. Data about the subject

2.1 Subject name	HDL-Based Digital Sefing						
2.2 Subject area	Electronic devices and circuits						
2.3 Course responsible/lecturer	Assoc.prof. Botond Sandor KIREI, PhD eng. botond.kirei@bel.utcluj.ro						
2.4 Teachers in charge of applications	Assoc.prof. Botond Sandor KIREI, PhD eng. botond.kirei@bel.utcluj.ro						
2.5 Year of study	II	2.6 Semester	1	2.7 Assessment	E	2.8 Subject category	DA/DI

3. Estimated total time

3.1 Number of hours per week	2	of which : 3.2 course	2	3.3 seminar / laboratory	1
3.4 Total hours in the curriculum	42	of which: 3.5 course	28	3.6 seminar / laboratory	14
Distribution of time					hours
Manual, lecture material and notes, bibliography					35
Supplementary study in the library, online specialized platforms and in the field					25
Preparation for seminars / laboratories, homework, reports, portfolios and essays					15
Tutoring					13
Exams and tests					6
Other activities:					

3.7 Total hours of individual study	83
3.8 Total hours per semester	125
3.9 Number of credit points	5

4. Pre-requisites (where appropriate)

4.1 Curriculum	Design of VLSI digital circuits, Systems with Digital Integrated Circuits, Systems with FPGA
4.2 Competence	VHDL or Verilog hardware description languages, integrated digital circuit and systems design

5. Requirements (where appropriate)

5.1. For the course	Amphitheater 368, Str. Baritiu, No. 26, Cluj Napoca

5.2. For the laboratories	Laboratory 501, Str. Observatorului, No. 2, Cluj Napoca

6. Specific competences

Professional competences	Theoretical knowledge, (What they need to know) • Boolean mathematics. Binary functions. Schannon decomposition. Binary trees. PCN notation (Positional Cube Notation). Boolean satisfiability. • Karnaugh charts for multivariable simplification. Minimization of logical functions with algebraic methods (Quine-McCluskey) and heuristic methods (knowledge of heuristic minimization operators) • Synthesis of combinational circuits in two floors. Multilevel minimization of logical functions • Mode of operation of simulators with infinitesimal time (delta-time). The modus operandi of simulators based on tact. • Basic digital circuits (logic gates, bistables, registers, sequential automata, memories) • Design flow of circuits dedicated to specific applications (ASIC) and programmable areas (FPGA) • Functional verification of the designed digital systems • Design for low consumption. Design for testability. Design knowledge according to the JTAG standard, for testability Acquired skills: (What he knows how to do) • Development of software tools for the representation of logical functions in binary trees. • Design of advanced digital circuits using VHDL and Verilog hardware description languages. Levels of abstraction. Transistor level description. Gate-level description. Description at the transfer level of the registers. System level description. Designing digital systems using the data and control path method (data/control path design) • Circuit verification using hardware verification languages (SystemC, SystemVerilog, Vera and E) and hardware verification libraries (Accelera Open Verification Library). The level of code coverage (Code Coverage). Verification methods (Unified Verification Method, Assertion Based Verification) Acquired skills: (What tools he knows how to use) • Knowledge of using programs dedicated to the design of digital circuits, such as the Methor Graphics ModelSim simulator. Using the Alliance design environment (synthesis of digital circuits in a standard cell technology, placement and routing, LVS verification) Knowledge of functional verification and code coverage using the Covered program.
Cross-competences	

7. Discipline objectives (as results from the key competences gained)

7.1 General objectives	Developing of programming/verification/testing skills.
7.2 Specific objectives	The purpose of this course is to develop an understanding of the technologies behind hardware design and verification. Students will develop an appreciation of the capabilities/limitations of various hardware design and verification methods. The course will cover the basics of VHDL / Verilog simulation and verification using formal techniques such as: symbolic simulation, boolean satisfiability and equivalence checking. The lectures will cover case studies of verification of complex digital systems, for example verification of low instruction set microprocessors

8. Contents

8.1 Lecture (syllabus)	Teaching methods	Notes

1. Introductory course. The design process using HDL 2. Combinational digital circuits (Karnaugh diagrams, simplification of logic functions, logic gates, memories) 3. Binary trees. PCN notation (Positional Cube Notation). Boolean satisfiability. 4. Sequential digital circuits (bistables, registers, sequential automata) 5. The "delta-time" simulators. Tact based simulators 6. Synthesis of combinational and sequential circuits 7. Modeling digital circuits with HDL 8. Designing a processor with a reduced instruction set 9. Modeling and synthesis of digital processing units (architecture of digital filters and adaptive filters) 10. The JTAG standard. Circuit design for testability 11. Hardware verification languages HVL (Hardware Verification Language): SystemVerilog, PSL 12. Code coverage level 13. Open Verification Library (OVL) 14. Assertions Based Verification	Presentation	.rojector
8.2 Laboratory	Teaching methods	Notes
15. Imposition of requirements (case study/feasibility) 16. Studying bibliographic references and existing solutions 17. Preparation of technical content 18. Presentation of preliminary results 19. Checking and improving the content 20. Developing a PowerPoint presentation 21. Final tests	Applications and presentations	computer, Xilinx Vivado Design Suite

Bibliography

1. *Botond Sandor Kirei, Proiectarea sistemelor digitale cu instrumente HDL, Casa Cartii de Stiinta, 2016*
2. *M. D. Ciletti, „Advanced Digital Design with the Verilog HDL", Ediția doua, Editura Prantice Hall, Upper Saddle River, New Jersey, 2011.*
3. *N. H. E. Weste, D. M. Harris, CMOS VLSI Design - A Circuits and Systems Perspective, Ediția patra, Editura Pearson Education, 2011*
4. *S. Kilts, „Advanced FPGA Design: Architecture, Implementation, and Optimization", Editura Wiley-IEEE Press, 2007*
5. *C.H. Roth, L. K. John, „Digital System Design Using VHDL", Ediția doua, Editura Thomson Learning, Toronto, Canada, 2008.*
6. *M. Zwolinski, „Digital System Design with SystemVerilog", Ediția Pearson Education, Crawfordsville, Indiana, 2009.*
   I. *Bucur, „Proiectare si Testare Logica", Editura Cartea Universitara, Bucuresti, 2006*
7. *S. Golson, „State Machine Design Techniques for Verilog and VHDL", Synopsys Journal of High-Level Design, pp. 1-2, 1994*
8. *S. Nicola, „Circuite Integrate Numerice. Aplicații în mecatronică", Ediția Universitaria, 2005*
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10. *Z. F. Baruch, „Structure of Computer Systems", Editura U. T. PRES, Cluj-Napoca, 2002*
11. *Z. F. Baruch, „Structura sistemelor de calcul", Editura Albastră, Cluj-Napoca, 2005*
12. *S. Hintea, „Tehnici de Proiectare cu Arii Logice", Editura U. T. Press, 2003*
13. *D. Nicula, Electronică digitală - Carte de învățătură, Ediția doua, Editura Universității Transilvania din Brașov, 2015*
14. *S. Iman, S. Joshi, „The e Hardware Verification Language", Editura Springer, 2004*

15. *L.M. Surhone, M. T. Tennoe, S. F. Henssonow, „OpenVera", Editura Betascript Publishing, 2011.*
16. *J. Bhasker, „A SystemC Primer, Second Edition", Editura Star Galaxy Publishing, 2004*
17. *B. S. Kirei, I. Dornean, A. Fazakas, M. Topa, "Comparing Verilog and VHDL", Proceedings of MicroCAD 2007, Miskolc, Hungary, pg. 35-40, 22-23 March 2007*
18. *Z. Hascsi, „Proiectarea Asistată de Calculator a Circuitelor Digitale", Notiție de curs, http://arh.pub.ro/zolih/courses/paccd/paccd.php, 22 Aprilie 2016 (ultima vizualizare)*
19. *Janick Bergeron, Eduard Cerny, Alan Hunter, Andrew Nightingale, „Verification Methodology Manual for Systemverilog", Springer, 2005*

9. Bridging course contents with the expectations of the representatives of the community, professional associations and employers in the field

The skills acquired will be necessary for employees who carry out their activity within the energy management services; the content of the discipline, together with the acquired skills and abilities, meet the expectations of the profile companies where the students are looking for a job

10. Evaluations

Activity type	10.1 Assessment criteria	10.2 Assessment methods	10.3 Weight in the final grade
10.4 Course	Theoretical knowledge	Exam	- E, max 10 pts 50%
10.5 Applications	Project work + PowePoint prezentation	Test	- L, max. 10 pts, 50%
10.6 Minimum standard of performance			
1. L ≥ 5 and E ≥ 5			

Date of filling in:	Responsible	Title Surname NAME	Signature
10.09.2022	Course	Assoc.prof. Botond Sandor KIREI, PhD eng.	
	Applications	Assoc.prof. Botond Sandor KIREI, PhD eng.	

Date of approval in the Department of Bases of Electronics

15.09.2022

Head of Bases of Electronics Department
Prof. Sorin HINTEA, PhD eng.

Date of approval in the Council of Faculty of Electronics, Telecommunications and Information Technology

21.09.2022

Dean
Prof. Ovidiu POP, PhD eng.