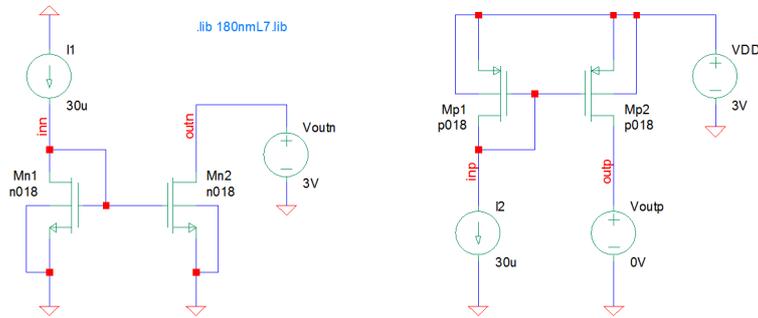


1. The fundamental current mirror with MOS transistors

The test schematic (*ogl-simpla-MOS.asc*):



Proposed exercises:

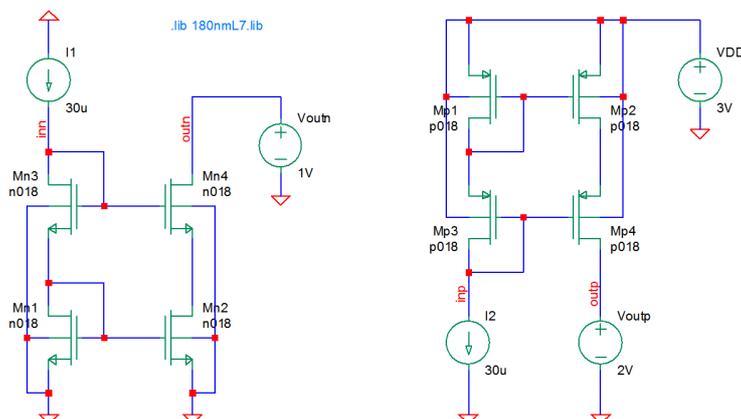
1. Size the transistors in the mirror for a current gain equal to unity, a $30\mu\text{A}$ input current and $V_{DSat} = 200\text{mV}$ for all devices.
2. Validate the operating points of the components and determine the input and the output resistances. Use the equations from the lecture notes and the small signal parameters returned by the simulation. Fill the following table for the NMOS transistors:

	V_{GS}	V_{DS}	I_D	V_{DSat}	V_{Th}	g_m	g_{DS}
M_{n1}							
M_{n2}							

3. Demonstrate through simulation that, if transistors are identical and the mirror is balanced in voltage ($V_{DS1} = V_{DS2}$), then all the errors of the current gain are cancelled.
4. Simulate the variation of the current gain ($n = I_D(Mn2)/I_D(Mn1)$) with the input-output voltage imbalance $V_{DS2} - V_{DS1} = V_{out} - V_{in}$.
5. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
6. Simulate the input characteristic and measure the input resistance around the bias point.
7. Repeat the exercises 1-6 for the PMOS implementation.

2. The cascode current mirror with MOS transistors

The test schematic (*ogl-cascoda-MOS.asc*):



Proposed exercises:

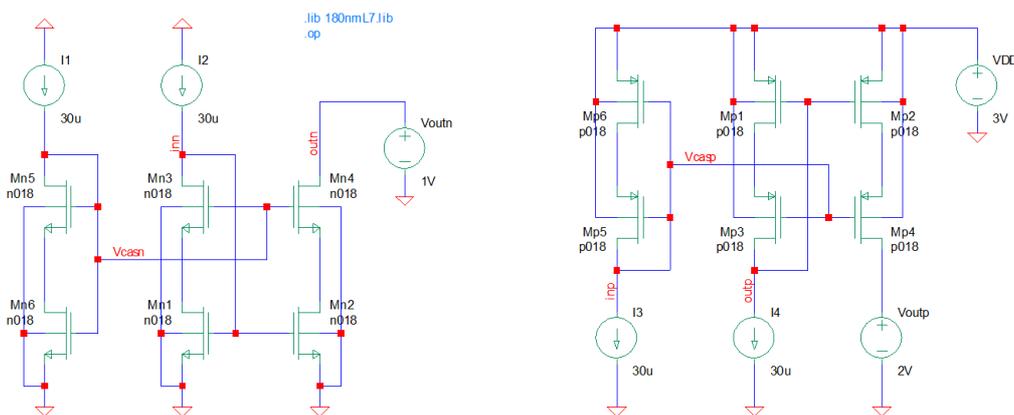
8. Size the transistors in the mirror for a current gain equal to unity, a $30\mu\text{A}$ input current and $V_{DSat}=200\text{mV}$ for all devices.
9. Validate the operating points of the components and determine the input and the output resistances. Use the equations from the lecture notes and the small signal parameters returned by the simulation. Estimate the minimum allowed output voltage and fill the following table for the NMOS transistors:

	V_{GS}	V_{DS}	I_D	V_{DSat}	V_{Th}	g_m	g_{DS}
M_{n1}							
M_{n2}							
M_{n3}							
M_{n4}							

10. Demonstrate through simulation that, if all transistors are identical, the current gain is approximately equal to unity, even when the input-output imbalance is not zero ($V_{in} \neq V_{out}$). What is the role of the cascode transistors in determining the current gain error?
11. Simulate the variation of the current gain ($n=I_D(Mn4)/I(I1)$) with the input-output voltage imbalance.
12. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
13. Simulate the input characteristic and measure the input resistance around the bias point.
14. Repeat the exercises 8-13 for the PMOS implementation.

3. The low swing cascode current mirror with MOS transistors

The test schematic (*ogl-cascodaLV-MOS.asc*):



Proposed exercises:

15. Size the transistors in the mirror for a current gain equal to unity, a $30\mu\text{A}$ input current and $V_{DSat}=200\text{mV}$ for all devices.

The sizing procedure takes into the account that all transistors, except M_{n6} , are biased in the saturation region. If the current gain is equal to unity, then the input and the output currents will be identical. Therefore, the current flowing through all transistors will be the same and equal to $30\mu\text{A}$. Since the V_{DSat} voltages must also be identical, all transistors will have the same geometry, determined by using the parameters associated with the reference operating point.

	I_D	W/L	V_{DSat}	V_{Th}
NMOS	$50\mu\text{A}$	$5\mu/1\mu$	240mV	450mV
PMOS	$50\mu\text{A}$	$15\mu/1\mu$	257mV	450mV

The scaling procedure of the bias point leads to the geometry for all the saturated devices:

$$\begin{cases} \frac{W}{L} = \left(\frac{W}{L}\right)_{ref} \cdot \frac{I_D}{I_{D-ref}} \cdot \left(\frac{V_{DSat-ref}}{V_{DSat}}\right)^2 = \frac{5}{1} \cdot \frac{30}{50} \cdot \left(\frac{240}{200}\right)^2 \cong \frac{4.3\mu}{1\mu} \\ AS = AD = W \cdot 0.2\mu = 0.86\text{pm}^2 \\ PS = PD = 2(W + 0.2\mu) = 9\mu\text{m} \end{cases}$$

The transistor M_{n6} is biased in the linear region, a constraint imposed by the topology of the circuit. The geometry of this device is determined by taking into account the equivalent drain-source resistance in the linear region. The voltage drop V_{DS6} across M_{n6} is approximately equal to V_{DS1} of the transistors M_{n1} and M_{n2} . The correct operation of the mirror requires M_{n1} and M_{n2} to be biased in saturation, which means that $V_{DS1} \geq V_{DSat1}$ and $V_{DS3} \geq V_{DSat3}$, while $V_{GS1} = V_{DS1} + V_{DS3}$. The gate-source voltage V_{GS1} of the transistor M_{n1} is then

$$V_{GS1} = V_{DSat1} + V_{Th1} = 200\text{mV} + 450\text{mV} = 650\text{mV}$$

The saturation condition for M_{n1} results

$$V_{DS1} > V_{DSat1} \Rightarrow V_{DS1} = 1.5 \cdot V_{DSat1} = 300\text{mV} \Rightarrow V_{DS3} = V_{GS1} - V_{DS1} = 350\text{mV}$$

Meanwhile, the gate potential of the cascode transistors is

$$\begin{aligned} V_{casn} &= V_{GS3} + V_{DS1} = V_{DSat3} + V_{Th3} + \Delta V + V_{DS1} = 200\text{mV} + 450\text{mV} + 100\text{mV} + 300\text{mV} = 1.05\text{V} \Rightarrow \\ \Rightarrow V_{DSat6} &= V_{GS6} - V_{Th6} = V_{casn} - V_{Th6} = 1.05\text{V} - 450\text{mV} = 600\text{mV} \end{aligned}$$

The voltage drops V_{DS1} , V_{DS2} and V_{DS6} are approximately equal due to the cascode transistors. Thus, the equivalent drain-source resistance of M_{n6} is defined by Ohm's law (applied only for transistors biased in the linear region where the device can be regarded as a resistor)

$$r_{DS6-lin} = \frac{V_{DS6}}{I_1} = \frac{300\text{mV}}{30\mu\text{A}} = 10\text{k}\Omega$$

Considering the equivalent resistance of a transistor in the linear region

$$r_{DS6-lin} = \frac{V_{DS}}{I_D} = \frac{L}{\mu C_{ox} W \left(V_{DSat} - \frac{V_{DS}}{2} \right)},$$

the geometry of the transistor is determined from

$$\frac{W_{n6}}{L_{n6}} = \frac{1}{\mu C_{ox} r_{DS6-lin} \left(V_{DSat6} - \frac{V_{DS6}}{2} \right)}$$

The process and material dependent product μC_{ox} is obtained from the reference parameters as

$$\mu C_{ox} = \frac{2I_{D-ref}L_{ref}}{W_{ref}V_{DSat-ref}^2} = 347 \frac{\mu A}{V^2}$$

Replacing all the parameters leads to $W_{n6}/L_{n6}=0.64=1.3\mu/2\mu$. The drain/source area and perimeters of the transistor M_{n6} are then $AS=AD=0.26\text{pm}^2$ and $PS=PD=3\mu\text{m}$.

16. Validate the operating points of all the transistors in the mirror. Adjust the geometries in order to match the simulated operating points with the design specifications. Fill the table with the specific parameters for each of the transistors.

The transistor biasing is validated through an operating point (.OP) analysis. After running the simulation, the output file (*View*→*Spice Error Log* or key combination *CTRL+L*) offers the required details bias point of the transistor M_{n6} , suggesting further adjustments of the geometry. By iteratively changing W_{n6} , L_{n6} , AS , AD , PS and PD until the voltages reach the hand calculated values, the geometry of M_{n6} results $W_{n6}/L_{n6}=1.8\mu/2\mu$, $AS=AD=0.36\text{pm}^2$ and $PS=PD=4\mu\text{m}$.

	V_{GS}	V_{DS}	I_D	V_{DSat}	V_{Th}	g_m	g_{DS}
M_{n1}	671mV	301mV	30 μ A	207mV	450mV	222 μ S	5.86 μ S
M_{n2}	671mV	304mV	30 μ A	207mV	450mV	222 μ S	5.67 μ S
M_{n3}	760mV	370mV	30 μ A	214mV	531mV	218 μ S	3.7 μ S
M_{n4}	757mV	696mV	30 μ A	211mV	532mV	221 μ S	2.63 μ S
M_{n5}	757mV	757mV	30 μ A	210mV	532mV	221 μ S	2.6 μ S
M_{n6}	1.06V	305mV	30 μ A	509mV	422mV	-	0.563 μ S

17. Determine the input and the output resistances. Use the equations from the lecture notes and the small signal parameters returned by the simulation. Estimate the minimum allowed output voltage V_{o-min} .

The input resistance is calculated according to

$$R_{in} \cong \frac{1}{g_{m1}} = \frac{1}{222\mu S} = 4.5\text{k}\Omega$$

The output resistance is

$$R_{out} = r_{DS2} + r_{DS4} + g_{m4}r_{DS2}r_{DS4} = \frac{1}{g_{DS2}} + \frac{1}{g_{DS4}} + \frac{g_{m4}}{g_{DS2}g_{DS4}} \cong 15.44\text{M}\Omega$$

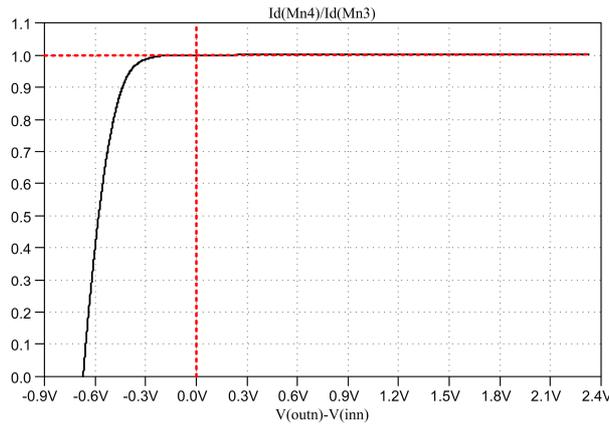
The minimum allowed output voltage is

$$V_{o-min} \cong V_{DSat2} + V_{DSat4} = 207\text{mV} + 211\text{mV} \cong 420\text{mV}$$

18. Simulate the variation of the current gain with the input-output voltage imbalance.

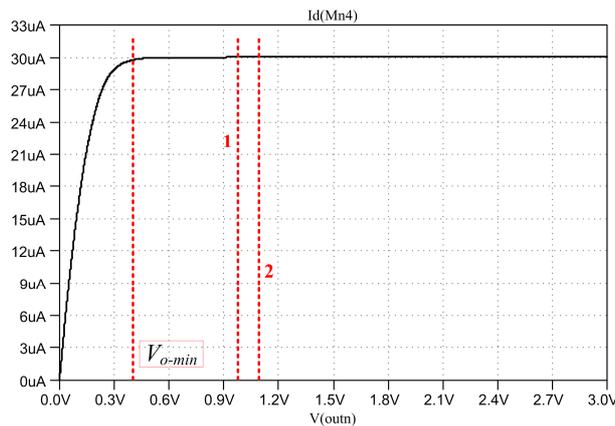
The current gain, defined as the ratio of the output current I_{out} to the input current I_{in} , is simulated by running a .DC analysis, in which the output voltage V_{outn} changes the output current while the input current remains constant. The simulation profile varies the source V_{outn} on a linear scale between 0V and 3V with a 1mV step size. The corresponding Spice command on the schematic will be *.dc Voutn 0 3 1m*.

After running the simulation, the current gain is plotted in the graphics windows as the ratio of the output current $I_{out}=I_d(M_{n4})$ and the input current $I_{in}=I_d(M_{n3})$. The variation of the current gain with the input-output voltage imbalance can be emphasized by changing the variable on the Ox axis with the difference $V(ou\text{tn})-V(in\text{n})$. The curve shows that the current gain is equal to unity when the mirror is balanced. Furthermore, the current gain is maintained at unity even for a non-zero voltage imbalance due to the cascode transistors that force the input and the output voltages of the fundamental mirror $M_{n1}-M_{n2}$ to be identical. For a negative voltage imbalance the output voltage violates the V_{o-min} requirement of the mirror. It results that the transistors M_{n2} and M_{n4} on the output branch cannot be correctly biased in the saturation region and the output current will exhibit a drop with V_{outn} instead of being constant.



19. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.

The output characteristic results from the simulation performed in the exercise 18 by swapping the variable on the Oy with the output current $I_d(M_{n4})$. The variable on the Ox axis must be the output voltage $V(ou\text{tn})$.



The output resistance is measured by placing the two cursors in two distinct locations around the operating point defined by the voltage $V_{outn}=1V$ and the current $I_{out}=30\mu A$. The measurement window shows the slope of the characteristic (*Slope*), while the output resistance is

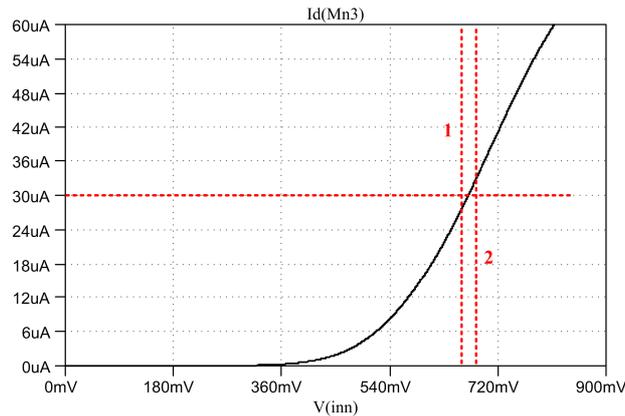
$$R_{out} = \frac{1}{Slope} \cong 19.6M\Omega$$

The difference compared to the value calculated by the simulator in the operating point analysis is given by the neglected substrate transconductance g_{mb4} of the transistor M_{n4} .

20. Simulate the input characteristic and measure the input resistance around the bias point.

Changing the source V_{outn} does not influence the input branch of the mirror. Thus, the input characteristic is simulated by varying the input current I_{in} provided by the source I_1 . The voltage source is swapped in the simulation profile with I_1 , changing between 0 and $60\mu\text{A}$ with a 10nA step size. The corresponding Spice command on the schematic sheet is then `.dc I1 0 60u 10n`.

In the first step after running the simulation the variable on the Oy axis is adjusted by plotting the input current $I_d(\text{Mn3})$. In the second step the variable on the Ox axis is changed to the input voltage $V(\text{inn})$.



The slope of the characteristic is measured by positioning the cursors at two distinct location around the operating point defined by the $30\mu\text{A}$ input current. Reading the slope of the curve in the measurement windows gives the input resistance according to

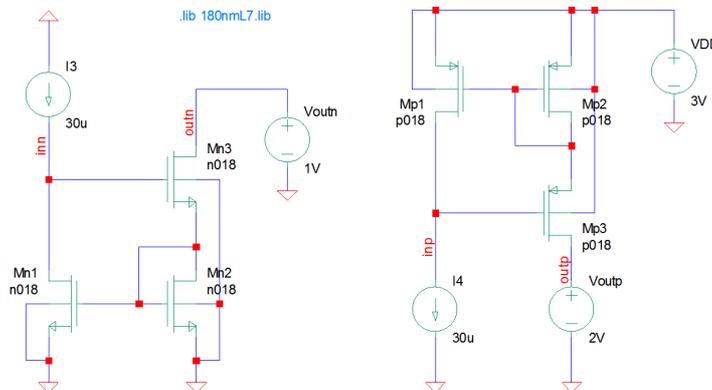
$$R_{in} = \frac{1}{\text{Slope}} = \frac{1}{g_{m1}} = \frac{1}{217\mu\text{S}} \cong 4.6\text{k}\Omega$$

The value of R_{in} found above corresponds to the one returned by the simulator in the operating point analysis. The precision of this measurement is strongly influenced by the distance between the cursors and the infinitely small variations of the transconductance ($\partial I_D / \partial V_{GS}$) around the bias point.

21. Repeat the exercises 15-20 for the PMOS implementation.

4. The asymmetrical Wilson current mirror with MOS transistors

The test schematic (`ogl-wilson-asim-MOS.asc`):



Proposed exercises:

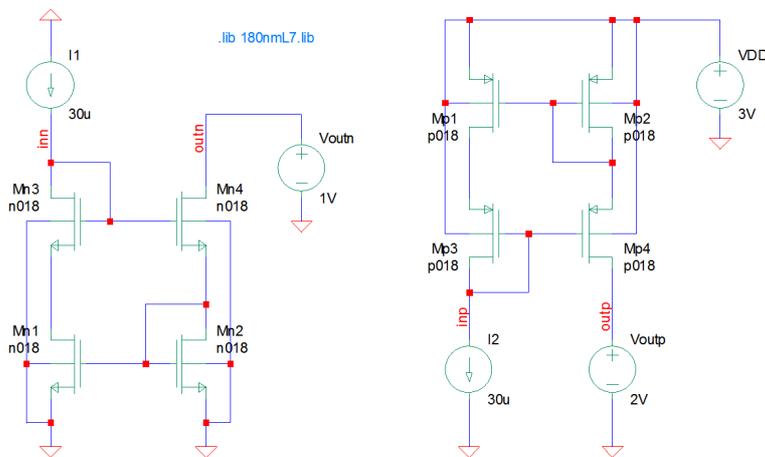
22. Size the transistors in the mirror for a current gain equal to unity, a $30\mu\text{A}$ input current and $V_{DSat} = 200\text{mV}$ for all devices.
23. Validate the operating points of the components and determine the input and the output resistances. Use the equations from the lecture notes and the small signal parameters returned by the simulation. Estimate the minimum allowed output voltage and fill the following table for the NMOS transistors:

	V_{GS}	V_{DS}	I_D	V_{DSat}	V_{Th}	g_m	g_{DS}
M_{n1}							
M_{n2}							
M_{n3}							

24. Demonstrate through simulation that, even if all transistors are identical and the input-output voltage imbalance is zero, the current gain exhibits a systematic error. Explain why.
25. Simulate the variation of the current gain ($n = I_D(Mn3)/I_D(Mn1)$) with the input-output voltage imbalance and observe the systematic error.
26. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
27. Simulate the input characteristic and measure the input resistance around the bias point.
28. Repeat the exercises 22-27 for the PMOS implementation.

5. The balanced Wilson current mirror with MOS transistors

The test schematic (*ogl-wilson-MOS.asc*):



Proposed exercises:

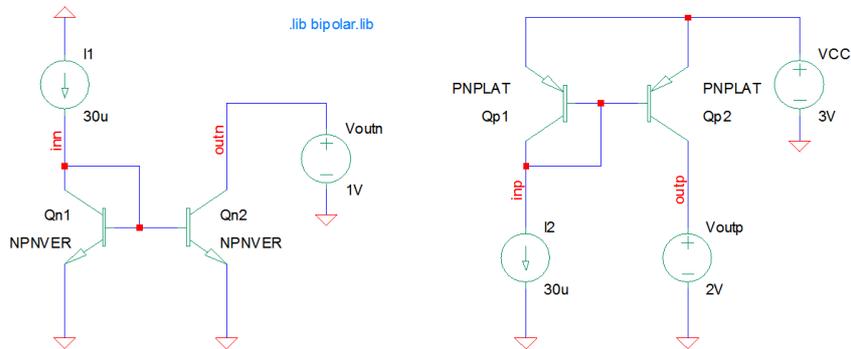
29. Size the transistors in the mirror for a current gain equal to unity, a $30\mu\text{A}$ input current and $V_{DSat} = 200\text{mV}$ for all devices.
30. Validate the operating points of the components and determine the input and the output resistances. Use the equations from the lecture notes. Estimate the minimum allowed output voltage and fill the following table for the NMOS transistors:

	V_{GS}	V_{DS}	I_D	V_{DSat}	V_{Th}	g_m	g_{DS}
M_{n1}							
M_{n2}							
M_{n3}							
M_{n4}							

31. Demonstrate through simulation that, if all transistors are identical, the current gain is approximately equal to unity, even when the input-output imbalance is not zero ($V_{in} \neq V_{out}$). What is the role of the cascode transistors in determining the current gain error?
32. Simulate the variation of the current gain ($n = I_{out}/I_{in}$) with the input-output voltage imbalance.
33. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
34. Simulate the input characteristic and measure the input resistance around the bias point.
35. Repeat the exercises 29-34 for the PMOS implementation.

6. The fundamental current mirror with bipolar transistors

The test schematic (*ogl-simpla-BJT.asc*):



Proposed exercises:

36. Simulate the operating points of the PNP transistors from the schematic. Fill the following table with the parameters of each device:

	V_{EB}	V_{EC}	I_C	I_B	β	g_m	r_{BE}	r_{CE}
Qp1	646mV	646mV	29.2μA	409nA	71.4	1.05mS	64kΩ	1.82MΩ
Qp2	646mV	1V	29.4μA	409nA	71.9	1.05mS	64kΩ	1.82MΩ

The operating points are simulated by running an *.OP* analysis. After creating the simulation profile and running the analysis the parameters of each transistor can be read from the output file.

37. Balance the input and the output voltages of the mirror and find the value of the device current gain β from the expression of n . Compare the result with the one from exercise 36.

The voltage balance of the mirror is achieved by matching the input and the output voltages. The simulated operating point shows that the input voltage of the mirror is $V_{in} = V_{EBp1}$, while the output voltage is $V_{out} = V_{ECp2}$. For the condition $V_{in} = V_{out}$ to be fulfilled, the source V_{outp} is adjusted to the value $V_{CC} - V_{in} = 3V - 646mV = 2.354V$. A new run of the *.OP* simulation gives the mirror current gain as

$$n = \frac{I_{out}}{I_{in}} = \frac{I_{Cp2}}{I_2} = \frac{29.18\mu A}{30\mu A} \cong 0.973$$

Considering the balanced input and output voltages ($V_{ECp1} = V_{ECp2}$), the expression of β is found from the dependence $n(\beta)$.

$$n = \frac{\beta}{\beta + 2} \Rightarrow \beta = \frac{2n}{1-n} = \frac{2 \cdot 0.973}{1-0.973} \cong 72.1$$

This value is close to the one found at the simulation of the operating point and filled in the table with the parameters of Q_{p1} and Q_{p2} .

38. Calculate the input and the output resistances by using the equations from the lecture notes and the simulated small signal parameters of the transistors.

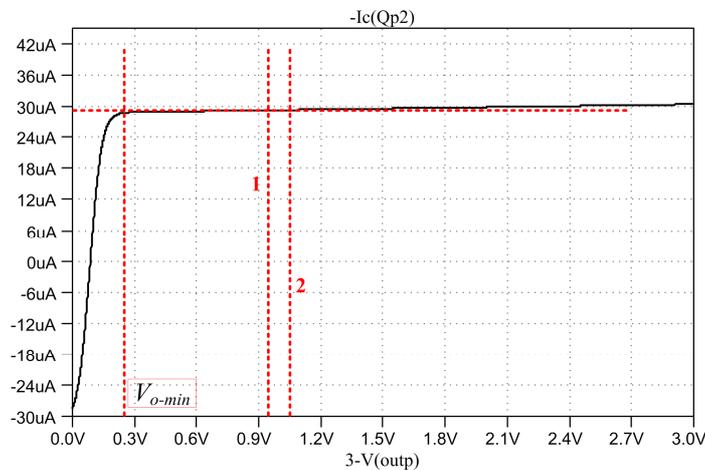
The output resistance of the mirror is found according to the expression

$$R_{in} \cong \frac{1}{g_{m1}} = \frac{1}{1.05\text{mS}} = 952\Omega$$

The output resistance is $R_{out}=r_{CE2}=1.82\text{M}\Omega$.

39. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.

The output characteristic is found with a *.DC* analysis in which the output voltage is varied on a linear scale. The source changed in the simulation profile will be V_{outp} , swept between 0V and 3V with a 1mV step size. The corresponding Spice command will be *.dc Voutp 0 3 1m*. After running the simulation the output current $-I_c(Qp2)$ is plotted in the graphics window. The negative sign is necessary due to the sign convention valid in every Spice simulator. Next, the variable on the O_x axis is changed to 3-V(outp).



Both cursors are then attached to the curve and positioned at two distinct spots around the 1V output voltage. The *Slope* parameter of the measurement window defines the output resistance as

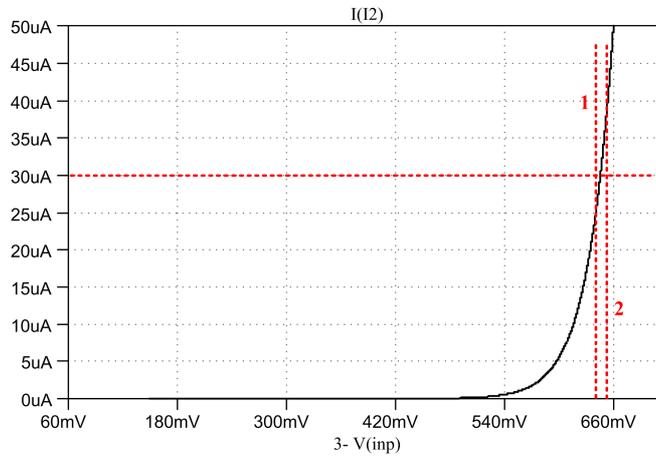
$$R_{out} = \frac{1}{Slope} \cong \frac{1}{0.546\mu\text{S}} = 1.83\text{M}\Omega$$

This value corresponds to the collector-emitter resistance of Q_{p2} found in the exercise 36.

40. Simulate the input characteristic and measure the input resistance around the bias point.

The input characteristic is again obtained through a *.DC* analysis, but this time the input current source I_2 is varied on a linear scale. In the simulation profile I_2 is swept between 0 and $50\mu\text{A}$ with a

10nA step size. The corresponding Spice command on the schematic will be `.dc I2 0 50u 10n`. After running the simulation, the input current I(I2) is plotted and then the *Ox* axis variable is change to 3-V(inp).



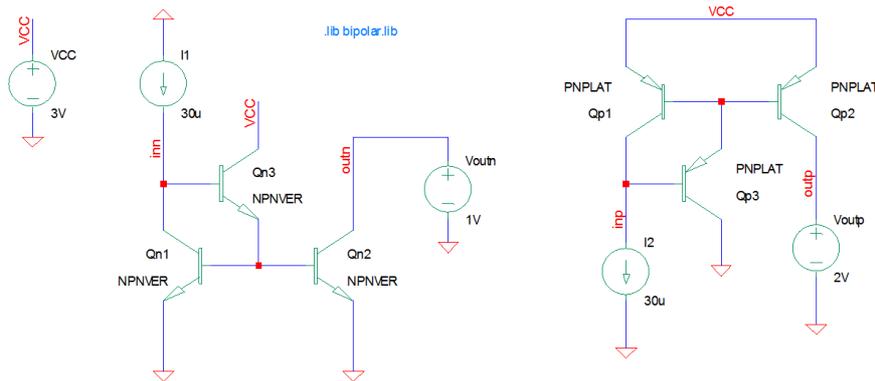
The input resistance is measured by zooming onto the region of the input characteristic containing the 30μA operating point and reading the *Slope* parameter from the measurement window. The calculated input resistance approximately corresponds to the one found from the small signal parameters in the exercise 37.

$$R_{out} = \frac{1}{Slope} = \frac{1}{g_{m1}} \cong \frac{1}{1.08\text{mS}} = 926\Omega$$

41. Repeat the exercises 36-40 for the NPN implementation.

7. The fundamental bipolar current mirror with β compensation

The test schematic (*ogl-efa-BJT.asc*):



Proposed exercises:

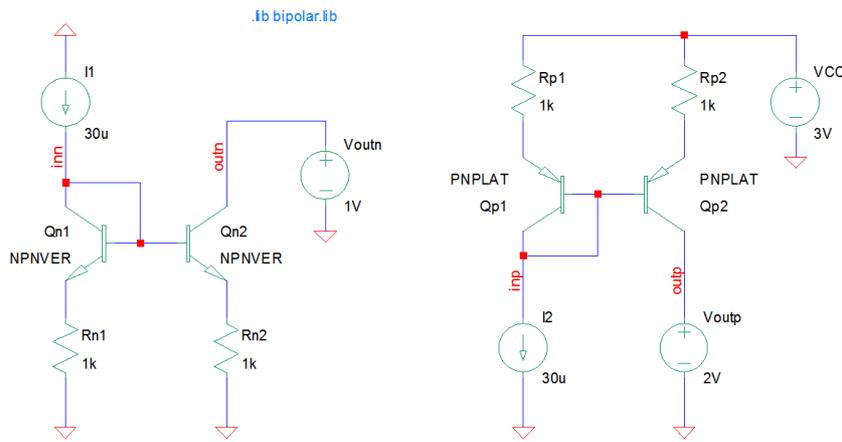
42. Simulate the operating points of the NPN transistors from the schematic. Fill the following table with the parameters of each device:

	V_{BE}	V_{CE}	I_C	I_B	β	g_m	r_{BE}	r_{CE}
Q _{n1}								
Q _{n2}								
Q _{n3}								

43. Balance the input and the output voltages and find the value of β from the current gain of the mirror. Compare the result with the value from the table in exercise 42.
44. Calculate the input and the output resistances by using the equations from the lecture notes and the simulated small signal parameters of the transistors.
45. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
46. Simulate the input characteristic and measure the input resistance around the bias point.
47. Repeat the exercises 42-46 for the PNP implementation.

8. The fundamental bipolar current mirror with resistive degeneration

The test schematic (*ogl-degR-BJT.asc*):



Proposed exercises:

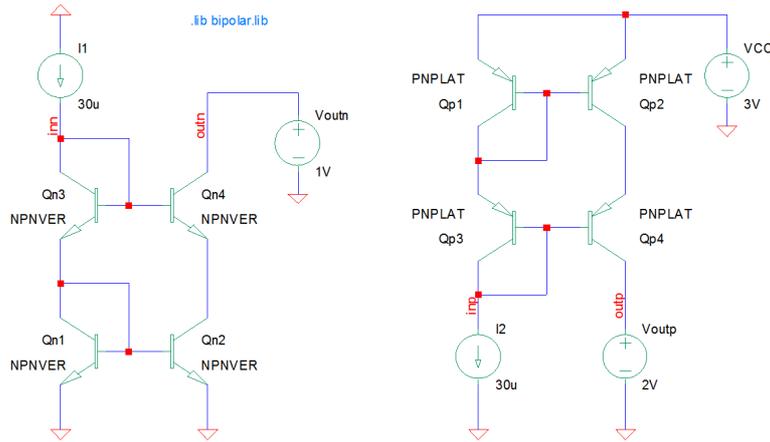
48. Simulate the operating points of the NPN transistors from the schematic. Fill the following table with the parameters of each device:

	V_{BE}	V_{CE}	I_C	I_B	β	g_m	r_{BE}	r_{CE}
Q _{n1}								
Q _{n2}								

49. Balance the input and the output voltages and find the value of β from the current gain of the mirror. Compare the result with the value from the table in exercise 48.
50. Calculate the input and the output resistances by using the equations from the lecture notes and the simulated small signal parameters of the transistors.
51. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
52. Simulate the input characteristic and measure the input resistance around the bias point.
53. Change the circuit in order to obtain a current gain equal to 2. *Hint*: the correct operation of the mirror requires equal current densities through both transistors.
54. Repeat the exercises 48-53 for the PNP implementation.

9. The bipolar cascode current mirror

The test schematic (*ogl-cascoda-BJT.asc*):



Proposed exercises:

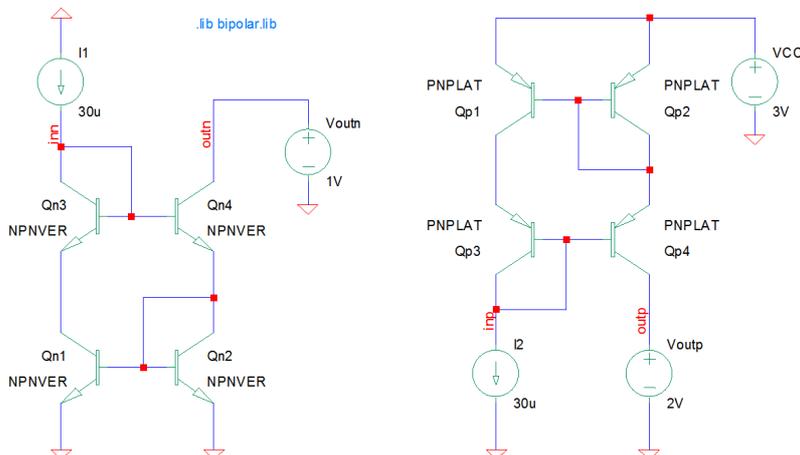
55. Simulate the operating points of the NPN transistors from the schematic. Fill the following table with the parameters of each device:

	V_{BE}	V_{CE}	I_C	I_B	β	g_m	r_{BE}	r_{CE}
Q _{n1}								
Q _{n2}								
Q _{n3}								
Q _{n4}								

- 56. Balance the input and the output voltages and find the value of β from the current gain of the mirror. Compare the result with the value from the table in exercise 55.
- 57. Calculate the input and the output resistances by using the equations from the lecture notes and the simulated small signal parameters of the transistors.
- 58. Simulate the variation of the current gain ($n=I_C(Qn4)/I(I1)$) with the input-output voltage imbalance and explain the results.
- 59. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
- 60. Simulate the input characteristic and measure the input resistance around the bias point.
- 61. Repeat the exercises 55-60 for the PNP implementation.

10. The balanced bipolar Wilson current mirror

The test schematic (*ogl-wilson-BJT.asc*):



Proposed exercises:

62. Simulate the operating points of the NPN transistors from the schematic. Fill the following table with the parameters of each device:

	V_{BE}	V_{CE}	I_C	I_B	β	g_m	r_{BE}	r_{CE}
Q _{n1}								
Q _{n2}								
Q _{n3}								
Q _{n4}								

63. Balance the input and the output voltages and find the value of β from the current gain of the mirror. Compare the result with the value from the table in exercise 62.
64. Calculate the input and the output resistances by using the equations from the lecture notes and the simulated small signal parameters of the transistors.
65. Simulate the variation of the current gain ($n=I_C(Qn4)/I(I1)$) with the input-output voltage imbalance and explain the results.
66. Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the V_{o-min} voltage.
67. Simulate the input characteristic and measure the input resistance around the bias point.
68. Repeat the exercises 62-67 for the PNP implementation.