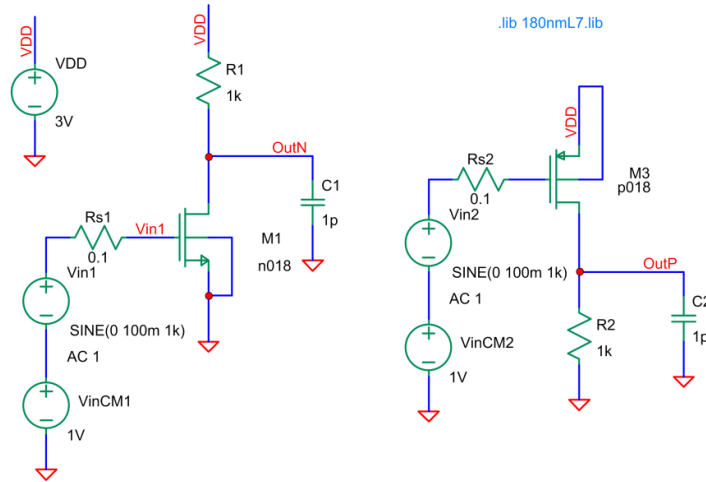


## 1. The common source amplifier with resistive load

The test schematic (*amp-sarcinaR.asc*):



### Proposed exercises:

- Design the amplifier for  $GBW > 20\text{MHz}$  and  $C_L = 1\text{pF}$ . In order to fulfill the design specifications in spite of the parasitic effects (capacitances,  $g_{mb}$ ), the parameters should be considered 1.5–2 times larger (for example, use  $GBW = 30\text{MHz}$  in hand calculations).

### Hints:

- from the expression of the unity-gain bandwidth ( $GBW$ ) calculate the small signal transconductance  $g_m$  of the input transistor;
  - choose a usual value for the  $V_{DSat}$  voltage of the input transistor (e.g. 200mV);
  - from the definition of the transconductance, a function of the drain current and the  $V_{DSat}$  voltage, determine the current flowing through the amplifier;
  - calculate the geometry  $W/L$  of the transistor by considering  $V_{DSat}$  and  $V_{Th}$ . Also determine the DC component of the input voltage  $V_{inCM1}$ , required for biasing;
  - choose the DC component  $V_{outDC}$  of the output voltage approximately equal to  $V_{DD}/2$  in order to maximize the output voltage swing and to avoid clipping;
  - from  $V_{outDC}$  and the current through the amplifier calculate the resistance  $R$ .
- Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

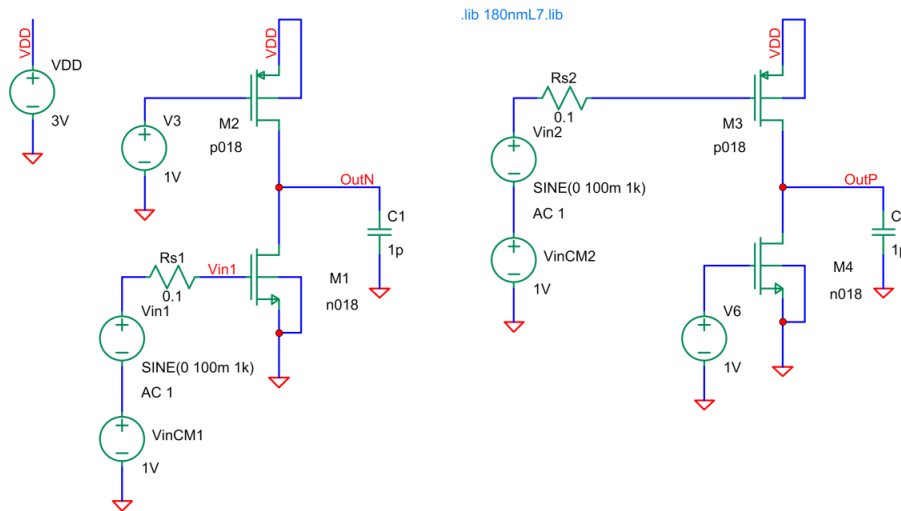
	$V_{GS}$	$V_{DS}$	$V_{Th}$	$V_{DSat}$	$I_D$	$g_m$	$r_{DS}$	$R$
M <sub>1</sub>								

- Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain  $A_0$  and the unity gain bandwidth  $GBW$  of the amplifier;
- Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic  $V_{out}/V_{in}$ ;
- Plot the magnitude and phase responses of the amplifier. Measure  $A_0$ , the frequency of the dominant pole ( $f_p = BW$ ) and the unity gain bandwidth  $GBW$ . Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations;

6. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 10mV and then 20mV. Measure the output amplitude for a 20mV input voltage? Is the output voltage clipped/distorted?
7. Repeat the exercises 1-6 for the same amplifier with a PMOS input transistor.

## 2. The common source amplifier with current source load

The test schematic (*amp-sarcinasrs.asc*):



### Proposed exercises:

8. Design the amplifier for  $GBW > 20\text{MHz}$  and  $C_L = 2\text{pF}$ . In order to fulfill the design specifications in spite of the parasitic effects (capacitances,  $g_{mb}$ ), the parameters should be considered 1.5–2 times larger (for example, use  $GBW = 30\text{MHz}$  in hand calculations).

### Hints:

- a. from the expression of the unity-gain bandwidth ( $GBW$ ) calculate the small signal transconductance  $g_m$  of the input transistor;
  - b. choose a usual value for the  $V_{DSat}$  voltage of the input transistor (e.g. 200mV);
  - c. from the definition of the transconductance, a function of the drain current and the  $V_{DSat}$  voltage, determine the current flowing through the amplifier;
  - d. calculate the geometry  $W/L$  of the transistors by considering  $V_{DSat}$  and  $V_{Th}$ . Also determine the DC component of the input voltage  $V_{inCM1}$  and the gate bias voltage of the load transistor ( $V_3$ );
  - e. choose the DC component  $V_{outDC}$  of the output voltage approximately equal to  $V_{DD}/2$  in order to maximize the output voltage swing and to avoid clipping;
9. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

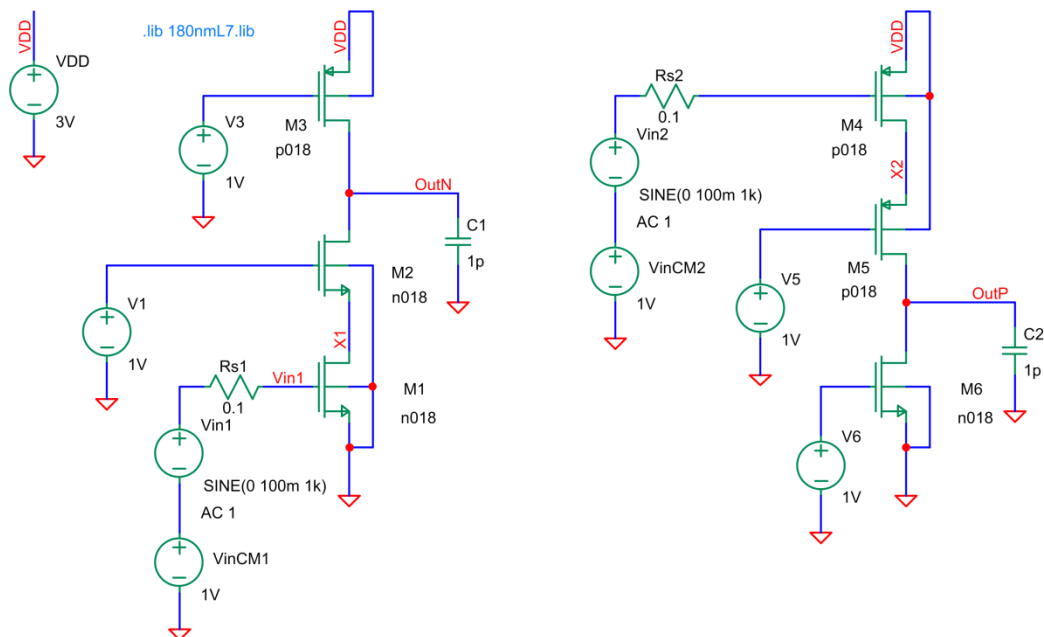
	$V_{GS}$	$V_{DS}$	$V_{Th}$	$V_{Dsat}$	$I_D$	$g_m$	$r_{DS}$
M <sub>1</sub>							
M <sub>2</sub>							

10. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain  $A_0$  and the unity gain bandwidth  $GBW$  of the amplifier;

11. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic  $V_{out}/V_{in}$ ;
12. Plot the magnitude and phase responses of the amplifier. Measure  $A_0$ , the frequency of the dominant pole ( $f_p=BW$ ) and the unity gain bandwidth  $GBW$ . Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations;
13. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 10mV and then 20mV. Measure the output amplitude for a 20mV input voltage? Is the output voltage clipped/distorted?
14. Repeat the exercises 8-13 for the same amplifier with a PMOS input transistor.

### 3. The common source amplifier with cascode input stage

The test schematic (*amp-cascoda.asc*):



#### Proposed exercises:

15. Design the amplifier for  $GBW > 20\text{MHz}$  and  $C_L = 1\text{pF}$ .

Designing the amplifier means the calculation of the bias voltages  $V_1$ ,  $V_3$ , of the DC input voltage  $V_{inCM1}$  and of all the transistor geometries from the design specifications

*In the first step* the unity-gain bandwidth ( $GBW$ ) is written as a function of the load capacitance. The equation leads to the required small signal transconductance of the amplifier ( $G_m$ ) which will be equal to the transconductance of the input transistor ( $g_{m1}$ ). In order to meet the design specifications in the presence of parasitic effects, the unity-gain bandwidth is typically designed to be 1.5-2 times larger than the lowest allowed value. Therefore, in calculations  $GBW = 30\text{MHz}$ .

$$GBW = \frac{G_m}{2\pi C_L} \Rightarrow G_m = g_{m1} = 2\pi C_L \cdot GBW = 2\pi \cdot 1 \cdot 10^{-12} \cdot 30 \cdot 10^6 = 188.5 \mu\text{S}$$

*In the second step* the  $V_{DSat}$  voltages of all the transistors are chosen to be a reasonable value, for example 200mV. The DC current flowing through the amplifier is then:

$$g_{m1} = \frac{2 \cdot I_D}{V_{DSat}} \Rightarrow I_D = \frac{g_{m1} \cdot V_{DSat}}{2} = \frac{188.5 \mu S \cdot 200 mV}{2} = 18.85 \mu A$$

In the third step the parameters of the reference operating point are used to scale the transistor geometries. The transistors  $M_1$  and  $M_2$  will be identical as they share the drain current and have the same  $V_{DSat}$  voltage.

$$\left(\frac{W}{L}\right)_{1,2} = \left(\frac{W}{L}\right)_{ref} \cdot \frac{I_D}{I_{D-ref}} \cdot \left(\frac{V_{DSat-ref}}{V_{DSat}}\right) = \frac{5}{1} \cdot \frac{18.85}{50} \cdot \left(\frac{240}{200}\right)^2 = \frac{2.71 \mu}{1 \mu}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_{ref} \cdot \frac{I_D}{I_{D-ref}} \cdot \left(\frac{V_{DSat-ref}}{V_{DSat}}\right) = \frac{15}{1} \cdot \frac{18.85}{50} \cdot \left(\frac{257}{200}\right)^2 = \frac{9.34 \mu}{1 \mu}$$

According to the width of each transistor, the drain/source diffusion area and perimeter will be

$$\begin{cases} AS_{1,2} = AD_{1,2} = 2.71 \mu m \cdot 0.2 \mu m = 0.54 \mu m^2 \\ PS_{1,2} = PD_{1,2} = 2 \cdot (2.71 \mu m + 0.2 \mu m) = 5.83 \mu m \\ AS_3 = AD_3 = 9.34 \mu m \cdot 0.2 \mu m = 1.87 \mu m^2 \\ PS_3 = PD_3 = 2 \cdot (9.34 \mu m + 0.2 \mu m) = 19.1 \mu m \end{cases}$$

In the fourth step the bias voltages  $V_1$  and  $V_3$  are determined from Kirchhoff's voltage law.

$$V_1 = V_{GS2} + V_{DS1} = V_{DSat2} + V_{Thn} + \Delta V_{Thn} + 1.5 \cdot V_{DSat1} = 200 mV + 446 mV + 100 mV + 300 mV = 1046 mV,$$

where  $V_{Thn}$  is the threshold voltage for  $V_{BS}=0V$ , while  $\Delta V_{Thn}$  compensates the increased threshold voltage of the cascode transistor due to the body effect. The  $1.5V_{DSat1}$  voltage is the drop across the transistor  $M_1$ .

$$V_3 = V_{DD} - V_{SG3} = V_{DD} - V_{DSat3} - V_{Thp} = 3V - 200 mV - 446 mV = 2.354V$$

Finally, the DC components of the input voltage ( $V_{inCM1}$ ) and of the output voltage ( $V_{outDC}$ ) can be calculated from the biasing requirements of the input transistor and from the maximized output voltage swing.

$$V_{inCM1} = V_{GS1} = V_{DSat1} + V_{Thn} = 200 mV + 446 mV = 646 mV$$

The output DC voltage is chosen to be approximately equal to  $V_{DD}/2$  in order to maximize the voltage range and avoid clipping. Consequently,  $V_{outDC}=1.5V$ .

16. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

	$V_{GS}$	$V_{DS}$	$V_{Th}$	$V_{DSat}$	$I_D$	$g_m$	$r_{DS}$
$M_1$	660mV	305mV	446mV	199mV	17.4 $\mu$ A	135 $\mu$ S	324k $\Omega$
$M_2$	741mV	1.2V	532mV	199mV	17.4 $\mu$	136 $\mu$ S	676k $\Omega$
$M_3$	707mV	1.5V	446mV	189mV	17.4 $\mu$	131 $\mu$ S	510k $\Omega$

The operating point of the transistors are verified by running an *.OP* analysis. The simulator returns 189mV for  $V_{DSat1}$ , while the drain-source voltage drop across  $M_1$  is approximately 109mV. It results that  $M_1$  is biased in the linear region. Furthermore, the DC component of the output voltage is 148mV which leads to the failure of the amplifier to operate correctly.

The adjustment of  $V_{DSat1}$  is done by changing  $V_{inCM1}$ , the final value being equal to 660mV. The DC output voltage can be set to 1.5V by iteratively adjusting the  $V_3$  voltage source. The final value found for  $V_3$  is 2.2929V.

17. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain  $A_0$  and the unity gain bandwidth  $GBW$  of the amplifier;

The low frequency gain is found according to the equation

$$A_0 = -G_m \cdot R_{out} \cong g_{m1} (r_{DS3} \parallel g_{m2} r_{DS2} r_{DS1}) \cong g_{m1} r_{DS3} = 135 \mu S \cdot 510 k\Omega = 68.8 \rightarrow 36.8 dB$$

The estimated bandwidth and unity-gain bandwidth will be

$$BW \cong \frac{1}{2\pi R_{out} C_L} = \frac{1}{2 \cdot \pi \cdot 510 k\Omega \cdot 1 pF} \cong 312 kHz$$

$$GBW \cong \frac{g_{m1}}{2\pi C_L} = \frac{135 \mu S}{2\pi \cdot 1 pF} \cong 21.5 MHz$$

18. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic  $V_{out}/V_{in}$ ;

The output voltage range is determined by evaluating the lowest voltage drop on the transistors

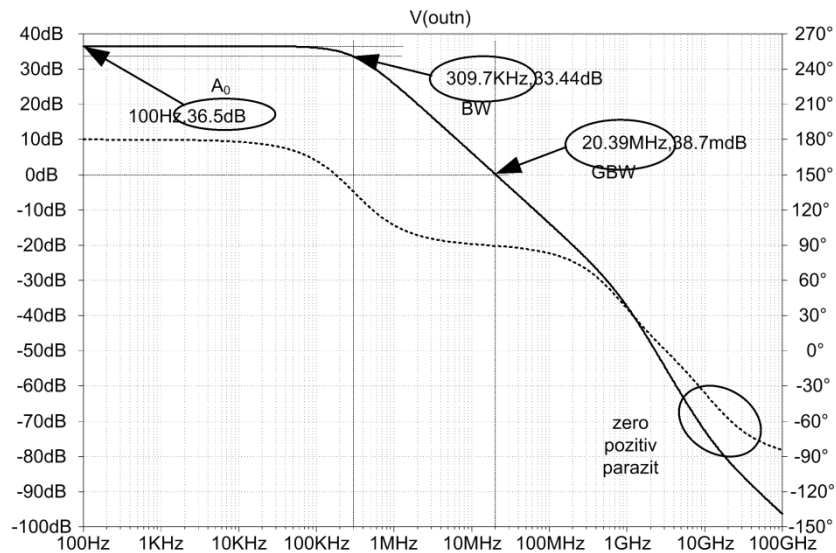
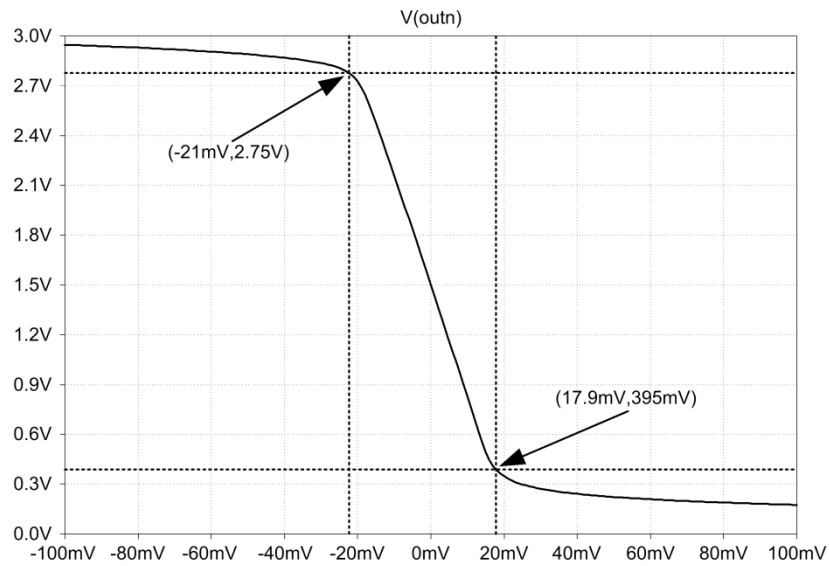
$$V_{OutN-\min} = V_{DSat1} + V_{DSat2} = 199 mV + 199 mV = 398 mV$$

$$V_{OutN-\max} = V_{DD} - V_{DSat3} = 3V - 189 mV = 2.811V$$

The largest output voltage swing can also be estimated by running a *.DC* analysis in which the input voltage, provided by the source  $V_{in}$ , is linearly changed between -100mV and 100mV with a 0.1mV step size. The corresponding Spice command on the schematic sheet will be *.dc Vin1 -100m 100m 0.1m*. The DC transfer characteristic of the amplifier is found by plotting V(OutN).

19. Plot the magnitude and phase responses of the amplifier. Measure  $A_0$ , the frequency of the dominant pole ( $f_p=BW$ ) and the unity gain bandwidth  $GBW$ . Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations;

The Bode diagrams corresponding to the amplifier are obtained by running an *.AC* analysis. The parameters of the analysis are chosen to visualize the important points on the frequency response. For example, if the estimated bandwidth and dominant pole frequency is 156kHz, the phase response will start dropping at around 15kHz. It results that the lower limit of the frequency range will be in the kHz region. Similarly, if the right half plane zero is located at high frequencies, the upper limit of the frequency range should be tens of GHz. Considering these limits, the frequency will be swept between 100Hz and 100GHz, with 100 point each decade. The corresponding Spice command is then *.ac dec 100 100 100G*.



For the measurement of the low frequency voltage gain the cursor is positioned on the flat section of the magnitude response and the  $O_y$  coordinate is read from the measurement window. It can be seen that the measured  $A_0$  gain is approximately 36.5dB, in accordance with the value calculated from the operating point and the small signal parameters.

The bandwidth is measured by placing the cursor to the point where the gain is 33.5dB or the phase is  $135^\circ$  on the phase axis. The bandwidth is defined as the frequency where the gain drops with 3dB or the phase drops with  $45^\circ$  compared to the low frequency values. Reading the parameters in the measurement window leads to a  $BW$  approximately equal to 310kHz.

The unity-gain bandwidth is defined as the frequency where the magnitude response intersects the  $O_x$  axis (where the gain becomes unity or 0dB). Placing the cursor to 0dB on the  $O_y$  axis gives a  $GBW$  approximately equal to 20.4MHz.

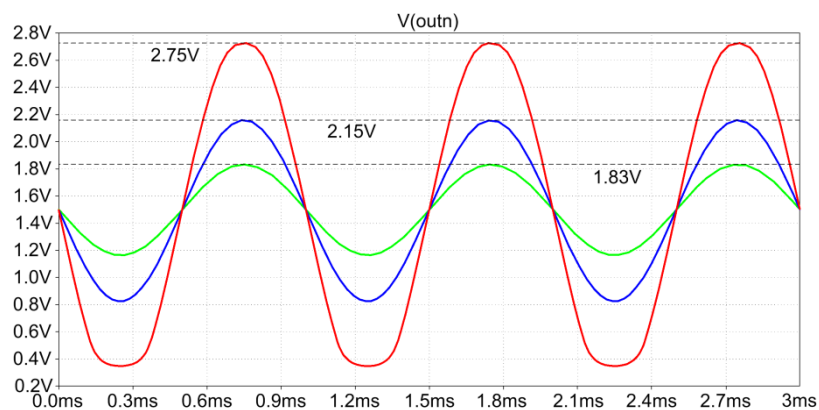
20. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 10mV and then 20mV. Measure the output amplitude for a 20mV input voltage? Is the output voltage clipped/distorted?

The time domain response of the amplifier is simulated by running a transient analysis that covers at least 3-4 complete periods of the signals. The frequency of the input signal should be sufficiently small in order to insure the full low frequency gain (the frequency should be on the flat section of the magnitude response). The maximum step size must be a compromise between accuracy

and simulation time. For linear circuits a good rule of thumb is to consider around 1000 point for each signal period. For a 1kHz input frequency the time range of the analysis can be limited to 3ms (3T) with the maximum step size 1 $\mu$ s. The corresponding Spice command is then `.tran 0 3m 0 1u`.

The parametric sweep required by the exercise imposes the definition of the input amplitude as parameter. Furthermore, the simulator must be instructed to run a transient analysis for every single input amplitude from the list. The additional parameter is defined by adding the Spice command `.param Ain=10mV` to the schematic (*Edit*  $\rightarrow$  *Spice Directive* or click on the `.op` icon in the menu bar), where *Ain* is the variable amplitude of the input signal. The parameter *Ain* can be associated with the input amplitude by changing the expression of the sine wave defined by the source  $V_{in}$  to `SINE(0 {Ain} 1k)`.

The transient analysis can be automatically run for every specified value of *Ain* if an additional command is placed on the schematic. The syntax of this command is `.step param Ain list 5m 10m 20m`. The `.STEP` command instructs the simulator to run a new transient analysis for every value of *Ain* and to save the plots resulting from each run.



The output amplitude resulting from each of the transient runs can be measured by choosing the *Select Steps* option of the *Plot Settings* menu and then individually plotting the output voltages resulting from the distinct runs of the transient analysis. The measured amplitudes for the signals without clipping are 1.83V for  $A_{in}=5\text{mV}$  (calculated as  $1.5\text{V}+A_{in}\cdot A_0$ ) and 2.15V for  $A_{in}=10\text{mV}$ . For larger input amplitudes the output voltage is clipped at around 2.75V and 380mV.

21. Repeat the exercises 15-20 for the same amplifier with a PMOS input transistor.

#### 4. The symmetrical cascode common source amplifier

The test schematic is `amp-cascoda-simetrica.asc`.

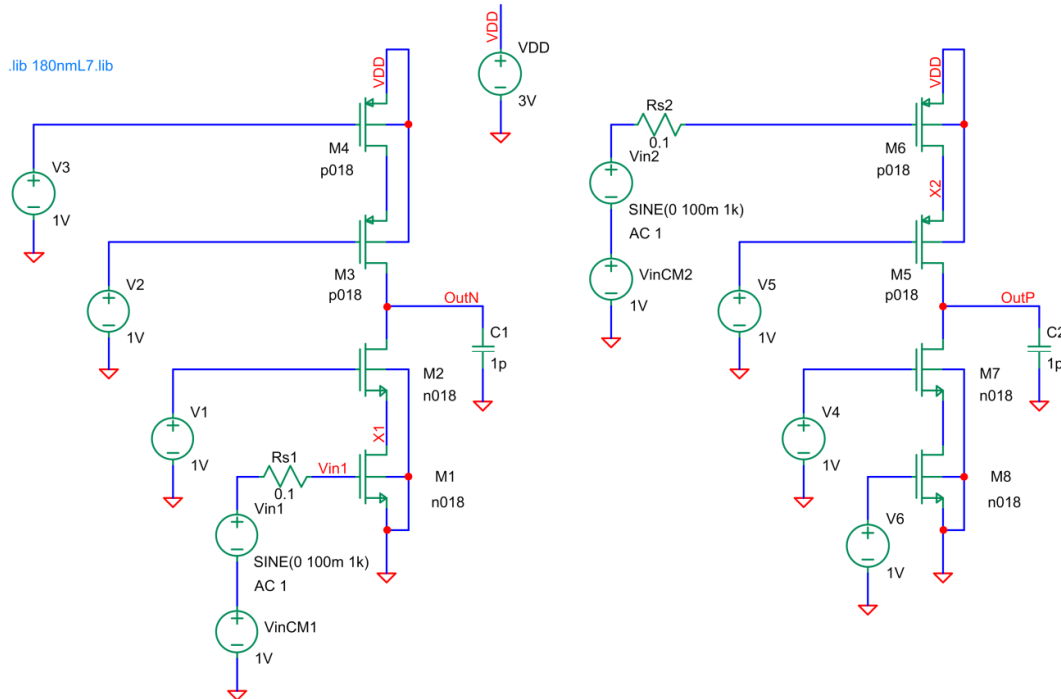
##### **Proposed exercises:**

22. Design the amplifier for  $GBW>20\text{MHz}$  and  $C_L=2\text{pF}$ . In order to fulfill the design specifications in spite of the parasitic effects (capacitances,  $g_{mb}$ ), the parameters should be considered 1.5–2 times larger (for example, use  $GBW=30\text{MHz}$  in hand calculations).

##### **Hints:**

- from the expression of the unity-gain bandwidth ( $GBW$ ) calculate the small signal transconductance  $g_m$  of the input transistor;
- choose a usual value for the  $V_{DSat}$  voltage of the input transistor (e.g. 200mV);
- from the definition of the transconductance, a function of the drain current and the  $V_{DSat}$  voltage, determine the current flowing through the amplifier;

- d. calculate the geometry  $W/L$  of the transistors by considering  $V_{DSat}$  and  $V_{Th}$ . Also determine the DC component of the input voltage  $V_{inCM1}$  and the gate bias voltages of the transistors ( $V_1, V_2, V_3$ );
- e. choose the DC component  $V_{outDC}$  of the output voltage approximately equal to  $V_{DD}/2$  in order to maximize the output voltage swing and to avoid clipping;



23. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

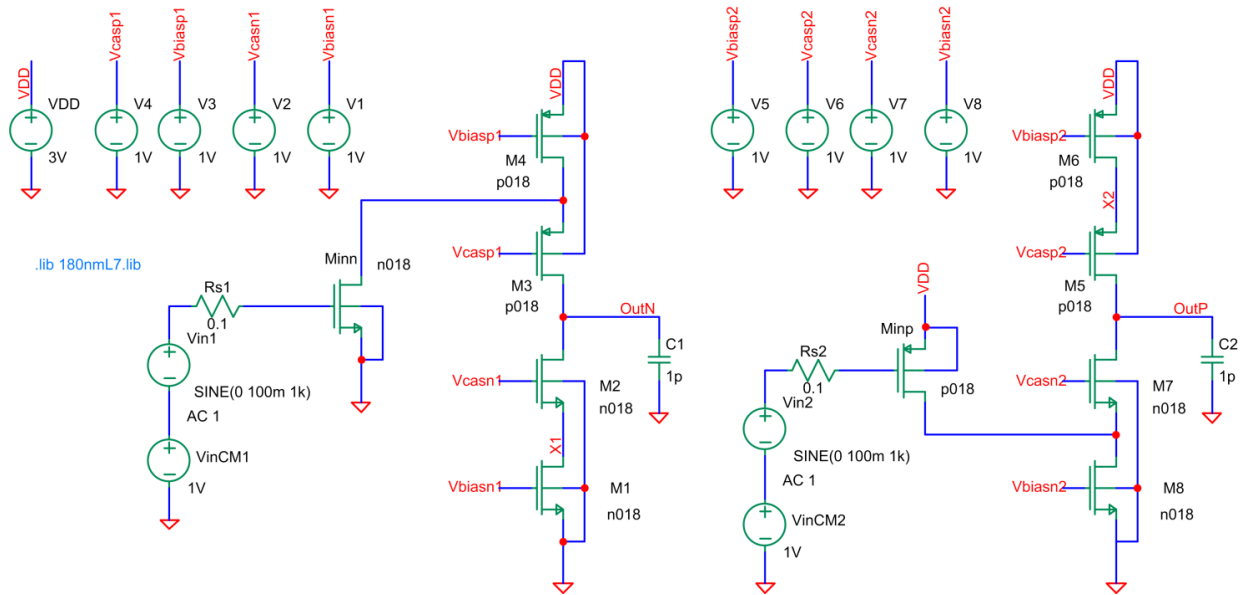
	$V_{GS}$	$V_{DS}$	$V_{Th}$	$V_{Dsat}$	$I_D$	$g_m$	$r_{DS}$
M <sub>1</sub>							
M <sub>2</sub>							
M <sub>3</sub>							
M <sub>4</sub>							

24. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain  $A_0$  and the unity gain bandwidth  $GBW$  of the amplifier;
25. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic  $V_{out}/V_{in}$ ;
26. Plot the magnitude and phase responses of the amplifier. Measure  $A_0$ , the frequency of the dominant pole ( $f_p=BW$ ) and the unity gain bandwidth  $GBW$ . Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations;
27. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 10mV and then 20mV. Measure the output amplitude for a 20mV input voltage? Is the output voltage clipped/distorted?
28. Repeat the exercises 22-27 for the same amplifier with a PMOS input transistor.

## 5. The folded cascode common source amplifier

The test schematic (*amp-cascoda-plitata.asc*):





**Proposed exercises:**

29. Design the amplifier for  $GBW > 20\text{MHz}$  and  $C_L = 2\text{pF}$ . In order to fulfill the design specifications in spite of the parasitic effects (capacitances,  $g_{mb}$ ), the parameters should be considered 1.5–2 times larger (for example, use  $GBW = 30\text{MHz}$  in hand calculations).

**Hints:**

- a. from the expression of the unity-gain bandwidth ( $GBW$ ) calculate the small signal transconductance  $g_m$  of the input transistor;
  - b. choose a usual value for the  $V_{DSat}$  voltage of the input transistor (e.g. 200mV);
  - c. from the definition of the transconductance, a function of the drain current and the  $V_{DSat}$  voltage, determine the current flowing through the input transistor. For simplicity, the current flowing through the folded output stage can be considered identical with the current through the input transistor;
  - d. calculate the geometry  $W/L$  of the transistors by considering  $V_{DSat}$  and  $V_{Th}$ . Also determine the DC component of the input voltage  $V_{inCM1}$  and the gate bias voltages of the transistors ( $V_{biasn1}$ ,  $V_{casn1}$ ,  $V_{casp1}$ ,  $V_{biasp1}$ );
  - e. choose the DC component  $V_{outDC}$  of the output voltage approximately equal to  $V_{DD}/2$  in order to maximize the output voltage swing and to avoid clipping;
30. Validate the operating points of the components and adjust the circuit to match hand calculations. Fill the following table:

	$V_{GS}$	$V_{DS}$	$V_{Th}$	$V_{DSat}$	$I_D$	$g_m$	$r_{DS}$
M <sub>inn</sub>							
M <sub>1</sub>							
M <sub>2</sub>							
M <sub>3</sub>							
M <sub>4</sub>							

31. Use the equations from the lecture notes and the small signal parameters to calculate the low frequency gain  $A_0$  and the unity gain bandwidth  $GBW$  of the amplifier;
32. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristic  $V_{out}/V_{in}$ ;

33. Plot the magnitude and phase responses of the amplifier. Measure  $A_0$ , the frequency of the dominant pole ( $f_p=BW$ ) and the unity gain bandwidth  $GBW$ . Notice the presence of the parasitic right half plane zero caused by the Miller effect and compare the measurements with the values found in hand calculations;
34. Simulate the transient response of the amplifier for a sine wave input with 1kHz frequency and the amplitude set to 5mV, 10mV and then 20mV. Measure the output amplitude for a 20mV input voltage? Is the output voltage clipped/distorted?
35. Repeat the exercises 29-34 for the same amplifier with a PMOS input transistor.