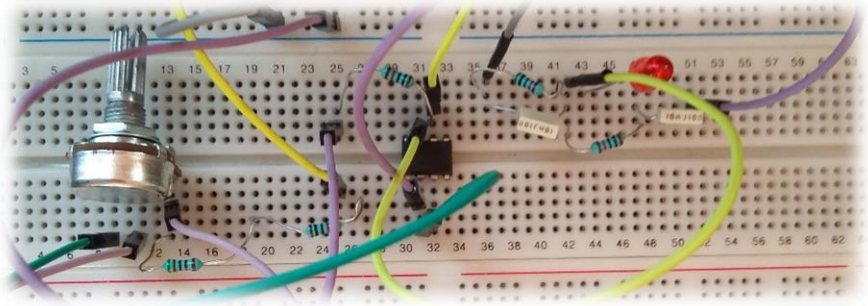


FUNDAMENTAL ELECTRONIC CIRCUITS

Assist. prof. Laura-Nicoleta IVANCIU, Ph.D.

C1 – Introduction. Transistors – recap. Transistor digital circuits.

Contents

- Course presentation
- Evaluation
- Transistors – recap
- Transistor digital circuits

Course presentation

Transistor digital circuits
- MOSFET digital circuits
- BJT digital circuits

Transistor amplifiers
- MOSFET basic amplifiers
- BJT basic amplifiers

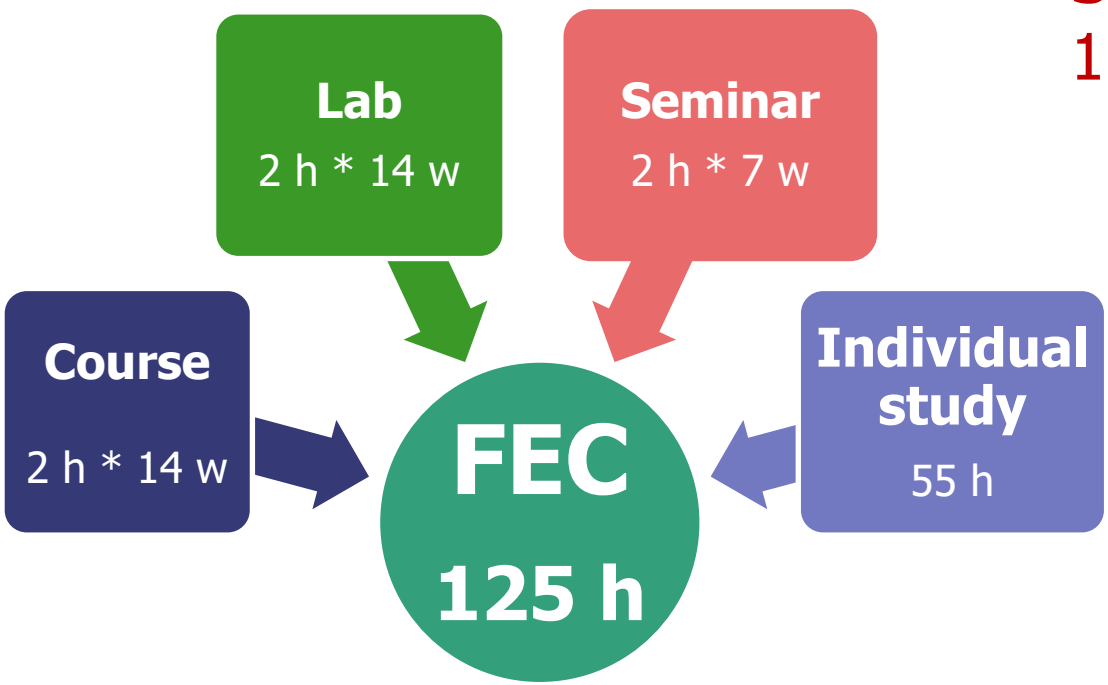
Power amplifiers
- Class A, B, AB

Feedback circuits
- Negative feedback
- Positive feedback

Voltage regulators
- Voltage regulators with OpAmp
- Integrated voltage regulators
- Switched-mode power supplies

Signal generators
- Sinusoidal signal generators
- Non-sinusoidal signal generators
- 555 Timer, class D amplifier

Time distribution



5 ECTS

125 h = 28 + 28 + 14 + 55

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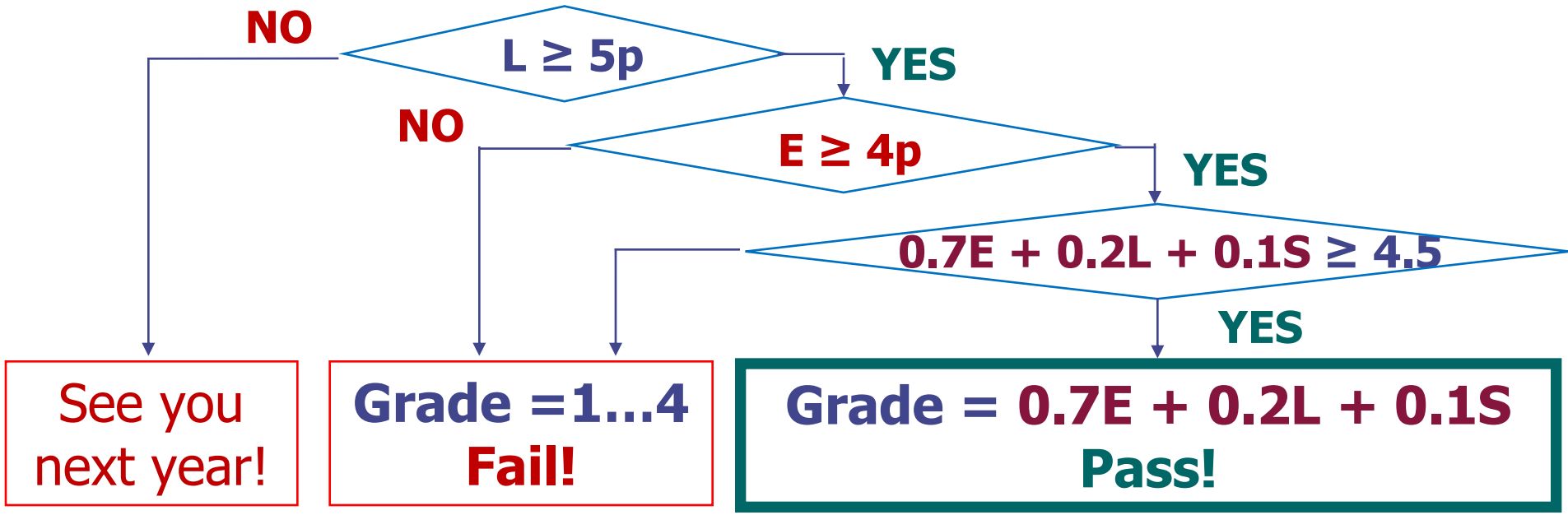
Evaluation

Written exam **(E)** 0…10 points	Lab **(L)** 0…10 points	Seminar **(S)** 0…10 points
• problem solving	• full attendance • activity • practical test	• full attendance • activity • problems - optional



Transistors - recap

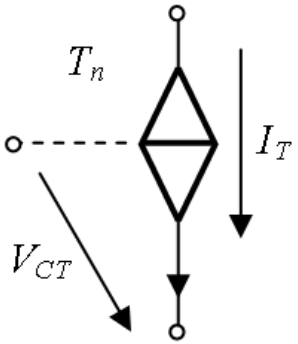
➢ Operating principle

transistors ≡ non-linear **voltage-controlled current sources**

square – MOSFET; exponential – BJT

n-type

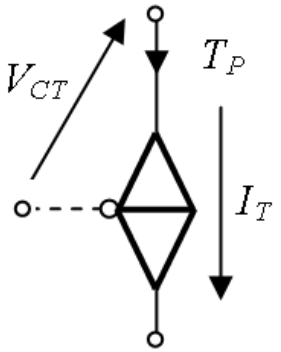
- n-channel MOSFET
- npn BJT



dc model – ideal VCCS

p-type

- p-channel MOSFET
- pnp BJT

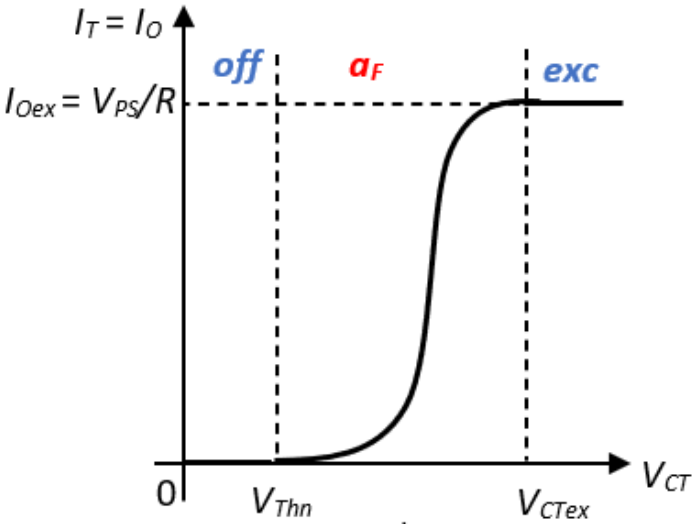


Transistors - recap

➢ Operating regions

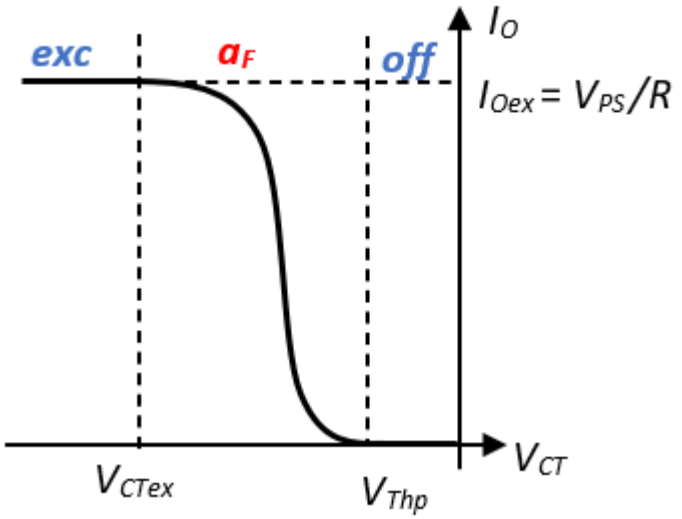
transistors ≡ non-linear **voltage-controlled current sources**

n-type



- $V_{CT} < V_{Thn}$, T_n – off, $I_T = 0$
- $V_{CT} > V_{Thn}$, T_n – on, $I_T > 0$

p-type



- $V_{CT} > V_{Thp}$, T_p – off, $I_T = 0$
- $V_{CT} < V_{Thp}$, T_p – on, $I_T > 0$

➢ Operating regions

- Two extreme regions, passive:

- **cutoff (off)**

$I_O = 0$; $V_O > 0$; ideal switch in off state

- **extreme conduction (exc)**

$I_O = I_{Oex}$; $V_O = 0$; ideal switch in on state

$V_{CT} < V_{Thn}$ or $V_{CT} > V_{CTex}$ - **switching transistor**

- An intermediate region, active:

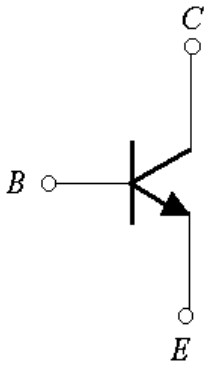
active forward region **(a_F)**

$V_{Thn} < V_{CT} < V_{CTex}$ – **permanent conduction (amplifier)**

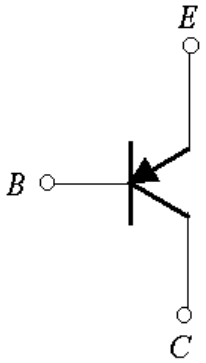
Transistors - recap

➢ Symbols

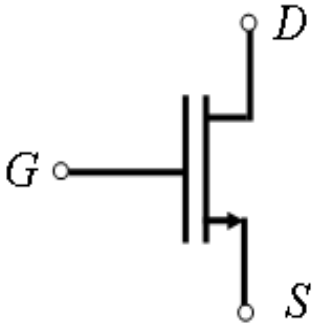
npn (n-type BJT)



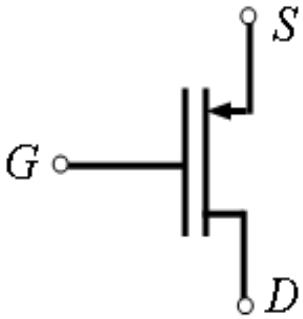
pnp (p-type BJT)



NMOS



PMOS



Transistor digital circuits

➢ To begin with

What is a logic/digital signal? How are these signal generated and measured?

Is a logic/digital circuit different from what we've studied so far?

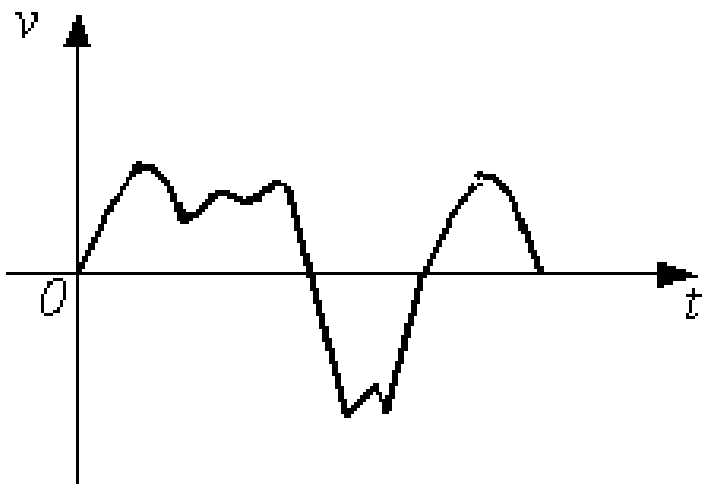
Are there special components, for logic/digital circuit use only?

Where are logic/digital signals and circuits used?

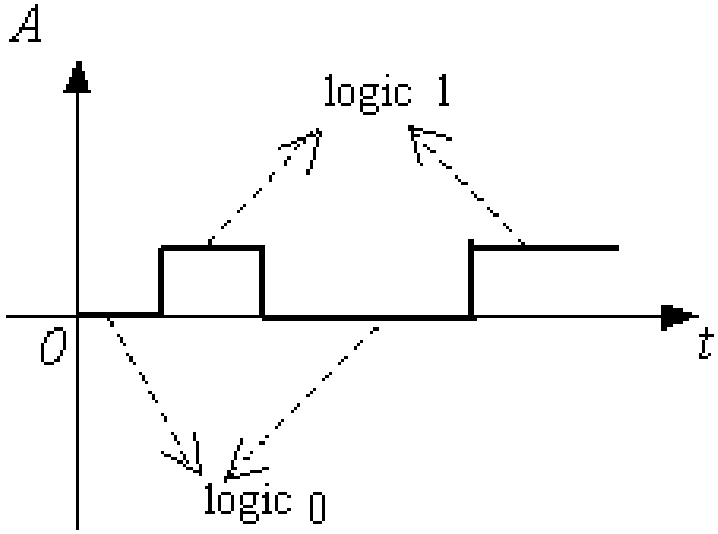
Transistor digital circuits

➢ Logic/digital signals

analog signal



digital signal



Logic 0 false/low

Logic 1 true/high

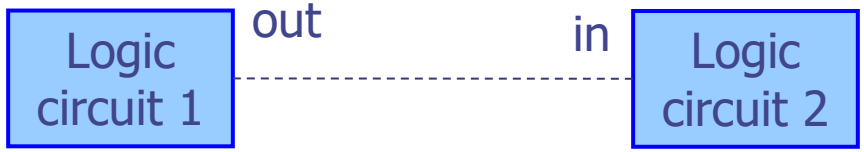
0 V → logic 0

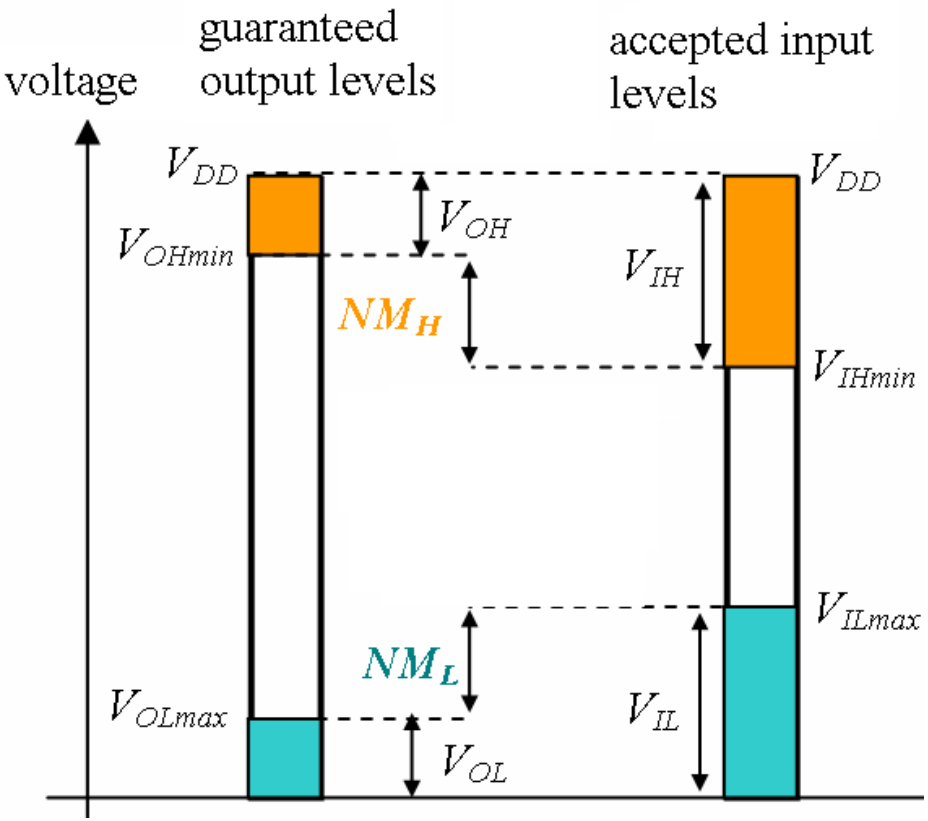
5 V or 10 V → logic 1

Accepted values?

Transistor digital circuits

➢ Noise margins





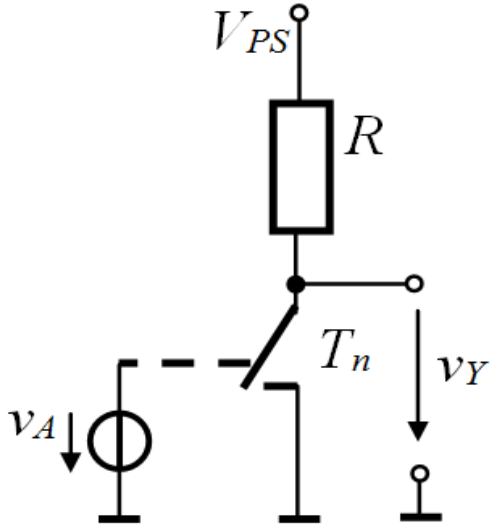
$$NM_H = V_{OH\,\min} - V_{IH\,\min}$$

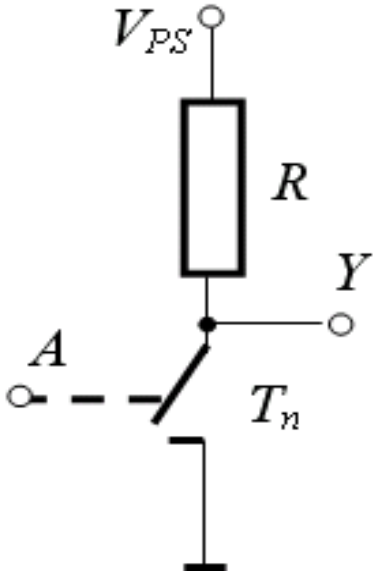
$$NM_L = V_{IL\,\max} - V_{OL\,\max}$$

Values?

Transistor digital circuits

➢ Logic inverters





v_A	T_n	v_y
0	off	V_{PS}
V_{PS}	on	0

Electrical operating table

0 V → logic 0 (Low)

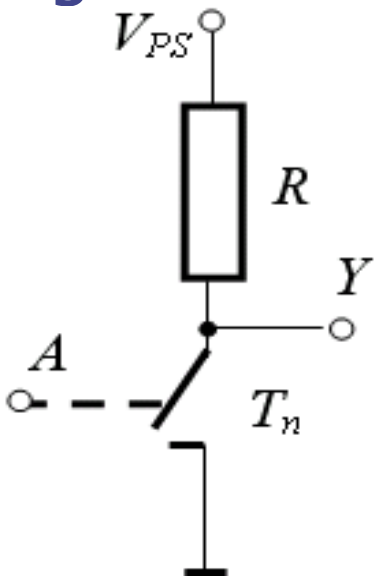
V_{PS} → logic 1 (High)

A	$Y = \overline{A}$
0	1
1	0

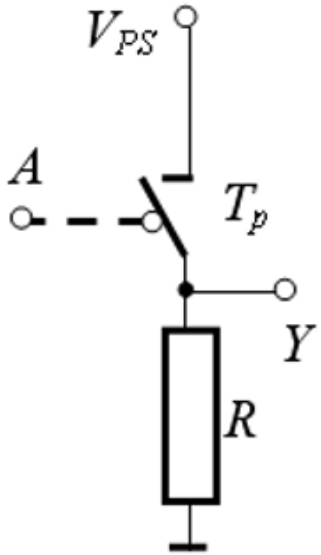
Truth/logic table

Transistor digital circuits

➢ Logic inverters



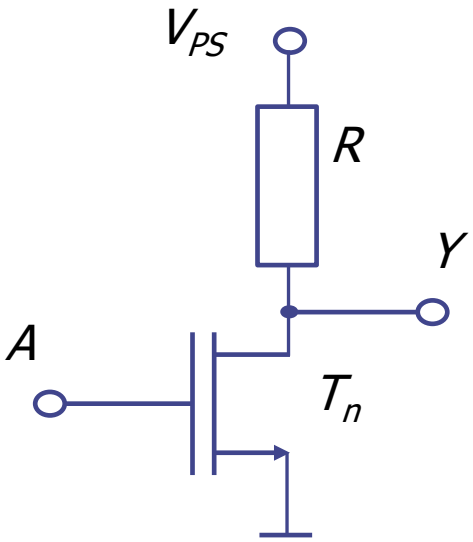
A	T_n	$Y = \overline{A}$
0	off	1
1	on	0



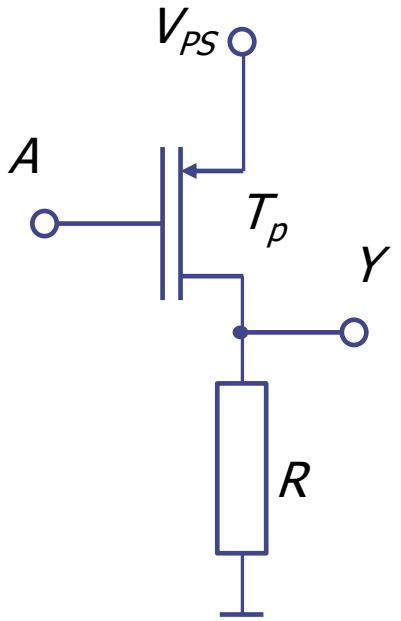
A	T_p	$Y = \overline{A}$
0	on	1
1	off	0

Transistor digital circuits

➢ Logic inverters – MOSFET and R



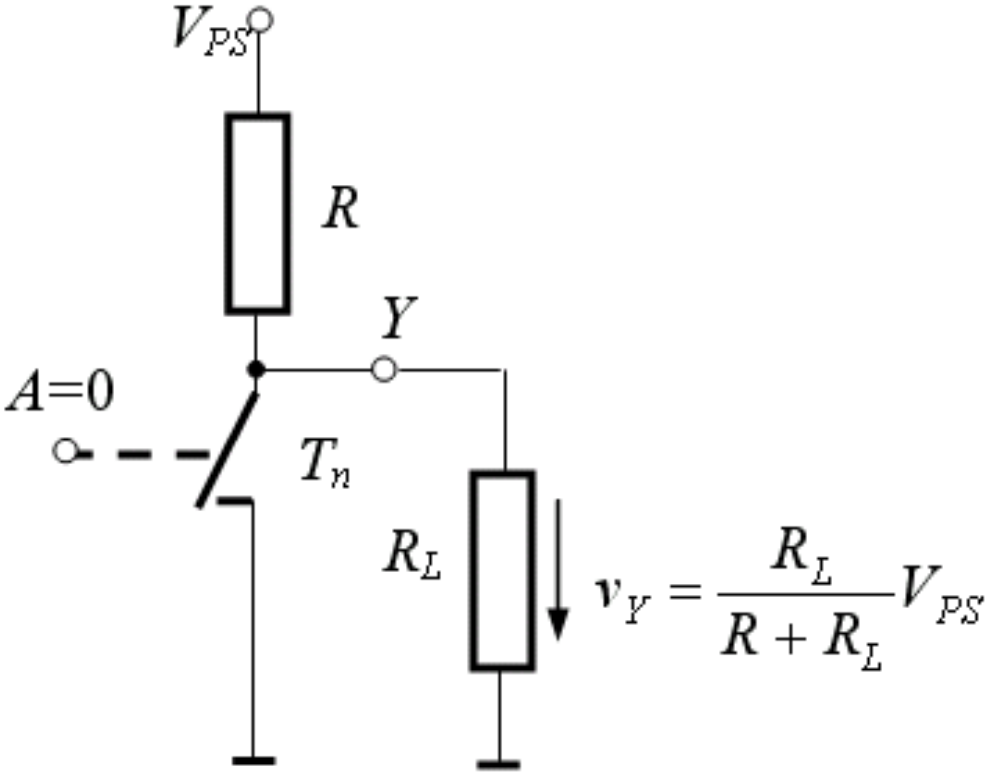
A	T_n	$Y = \overline{A}$
0	off	1
1	on	0

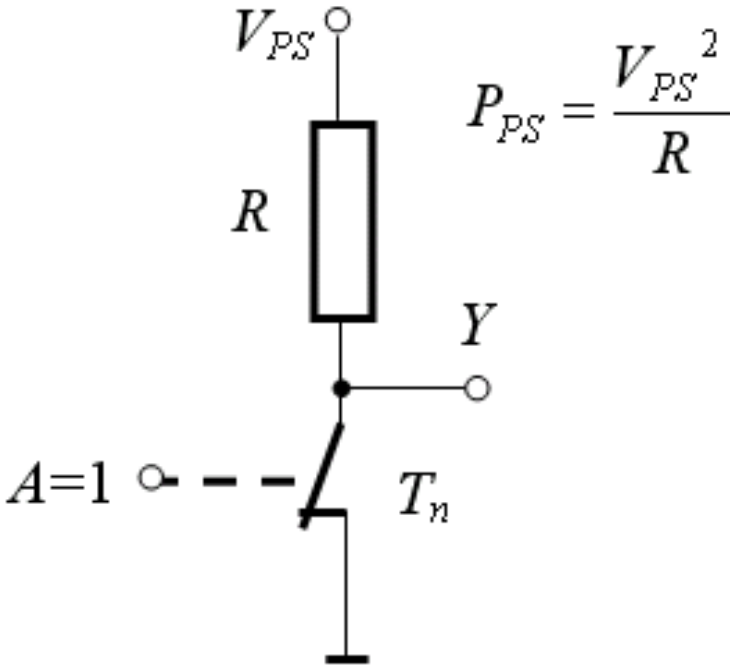


A	T_p	$Y = \overline{A}$
0	on	1
1	off	0

Transistor digital circuits

➢ Critical analysis of the logic inverter w/ T_n and R





Disadvantage elimination:

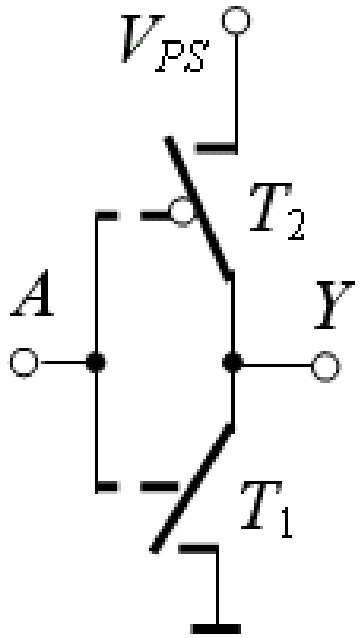
R as small as possible, ideally $R \to 0$

R as big as possible, ideally $R \to \infty$

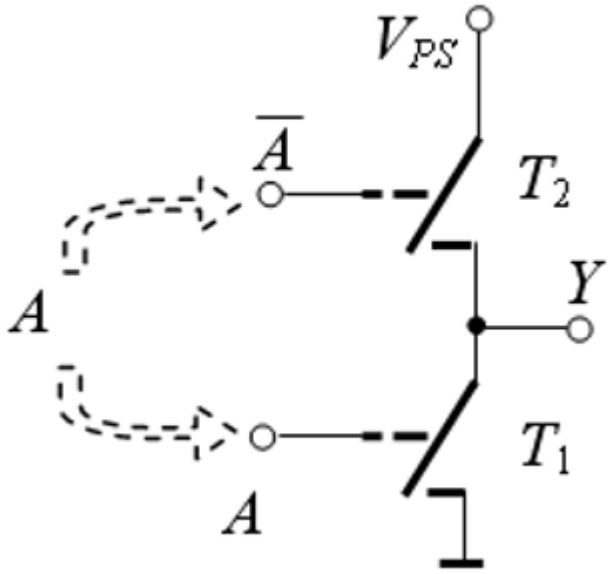
Solution?

Transistor digital circuits

➢ Solutions



A	T_1	T_2	$Y = \overline{A}$
0	off	on	1
1	on	off	0



complementary **switches**

Built w/: MOS transistors

CMOS (complementary MOS)

complementary **inputs**

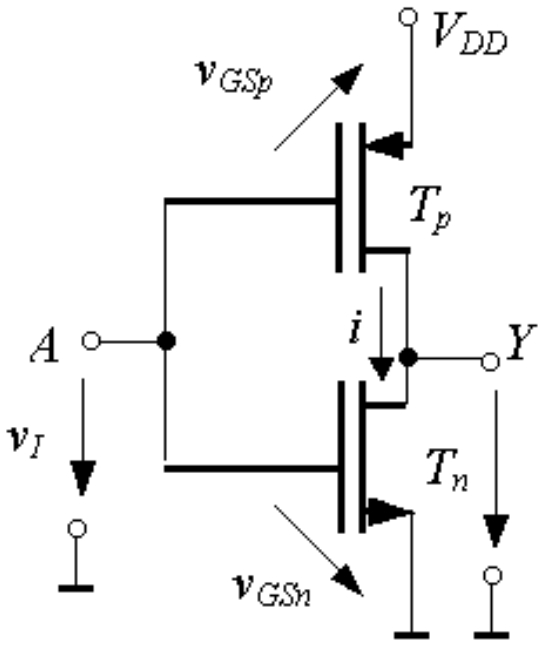
Built w/: BJTs and R

TTL (Transistor-Transistor Logic)

RTL (Resistor-Transistor Logic)

Transistor digital circuits

➢ CMOS logic inverter



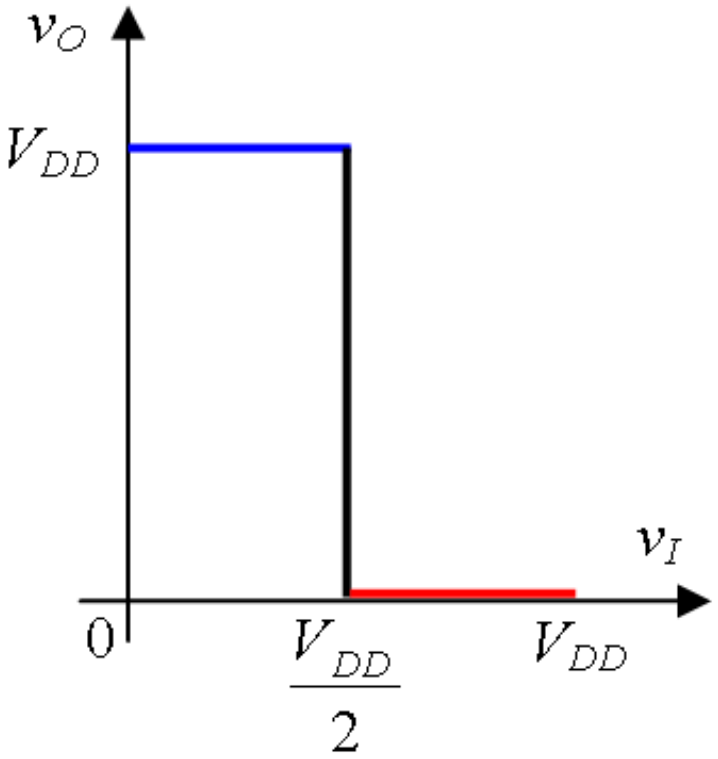
$$v_{GSn} = v_{Gn} - v_{Sn} = v_I$$
$$v_{GSp} = v_{Gp} - v_{Sp} = v_I - V_{DD}$$

v_I	v_{GSn}	T_n	v_{GSp}	T_p	v_O
0	$0 < V_{Thn}$	off	$-V_{DD} < V_{Thp}$	on	V_{DD}
V_{DD}	$V_{DD} > V_{Thn}$	on	$0 > V_{Thp}$	off	0

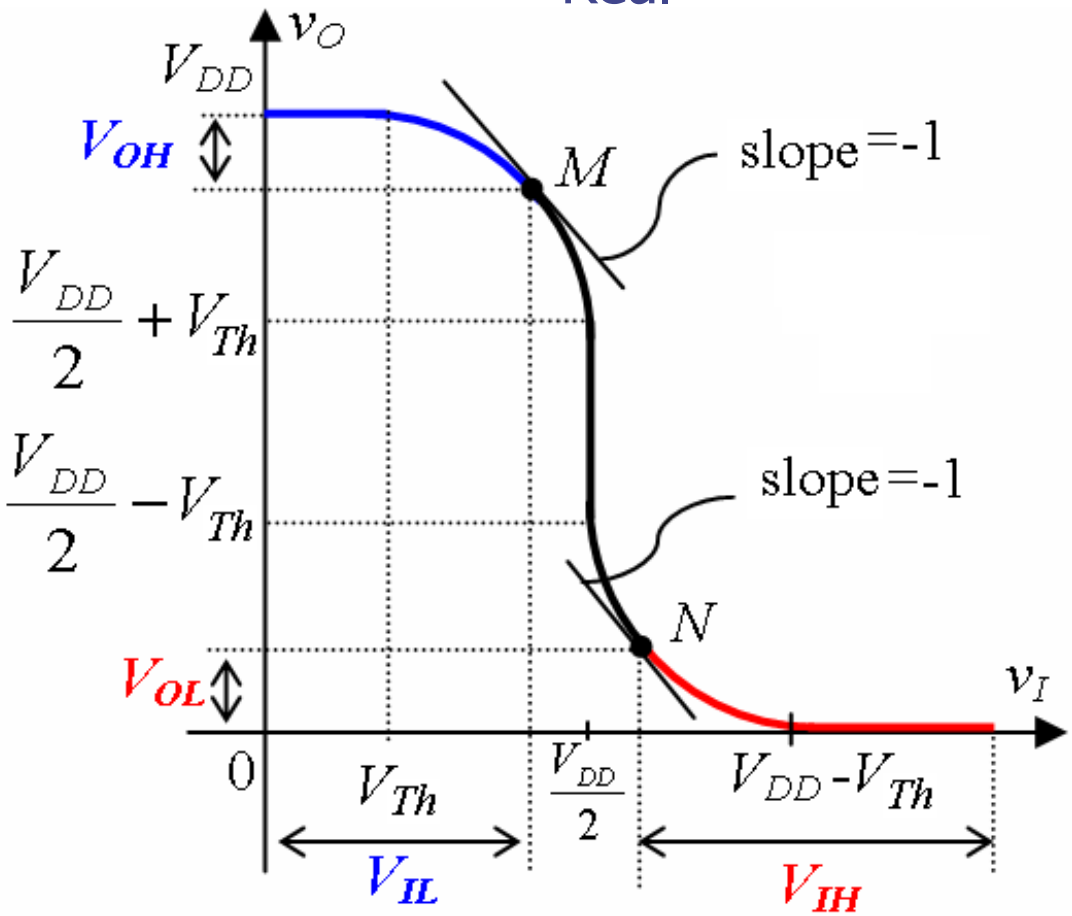
$$\boldsymbol{Y = \overline{A}}$$

➢ CMOS logic inverter – transfer characteristic

Ideal

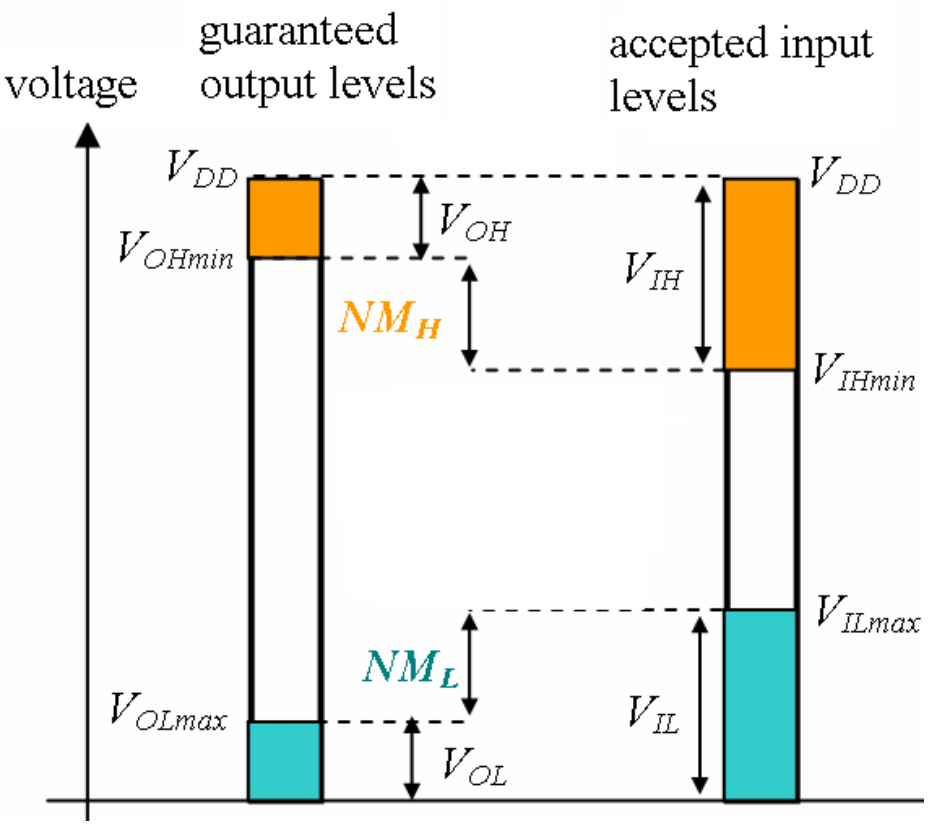


Real



Transistor digital circuits

- Noise margins for the CMOS logic family, 5 V supply

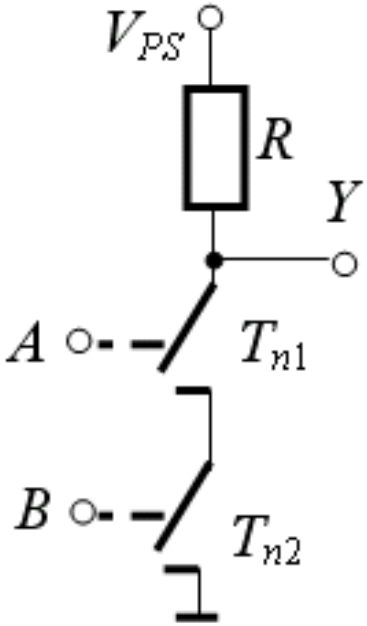


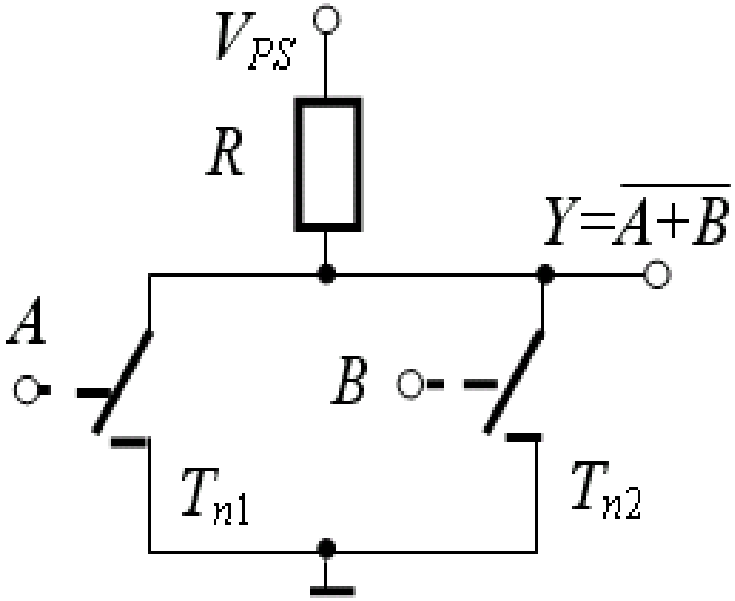
$$NM_H = 4.5 - 3.5 = 1\,V$$

$$NM_L = 1.5 - 0.5 = 1\,V$$

Transistor digital circuits

➢ Logic NAND, NOR – concept circuits

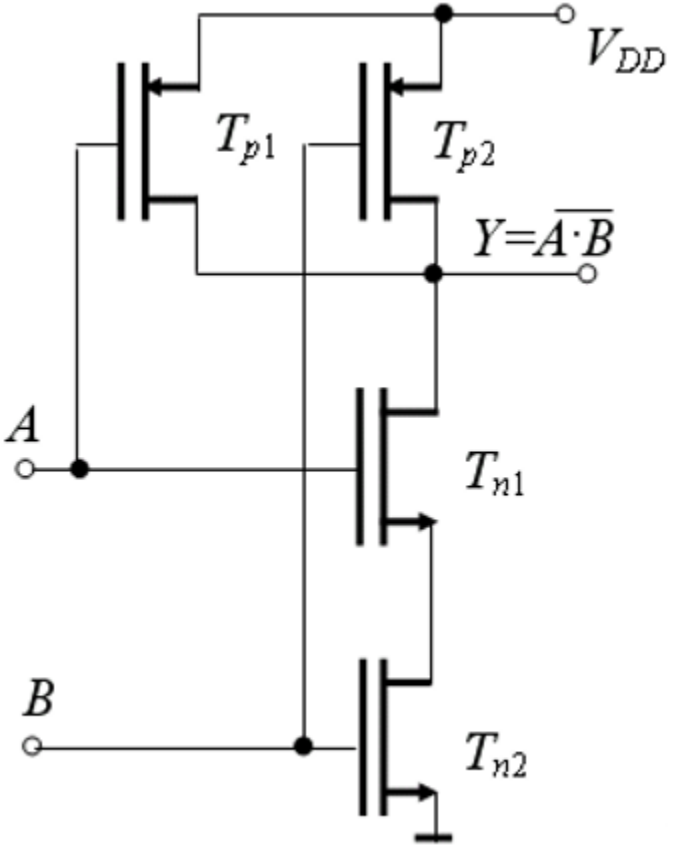


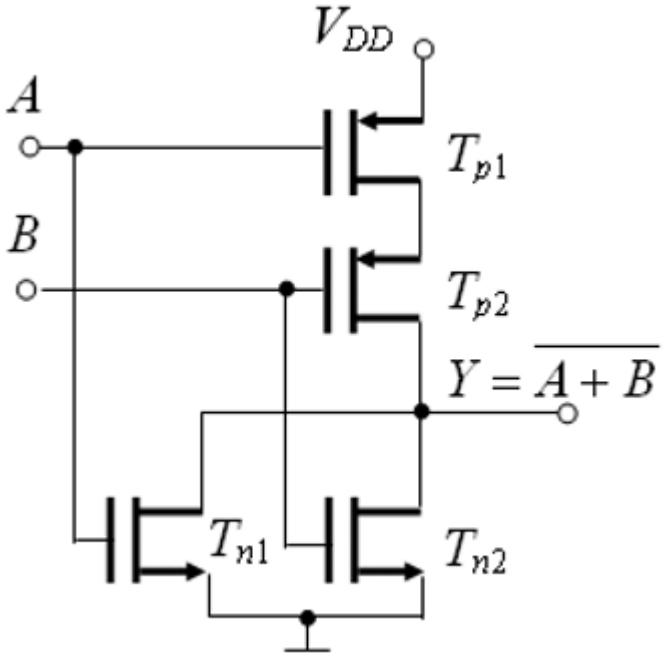


Truth tables?
How do we get rid of R?

Transistor digital circuits

- CMOS logic NAND, NOR

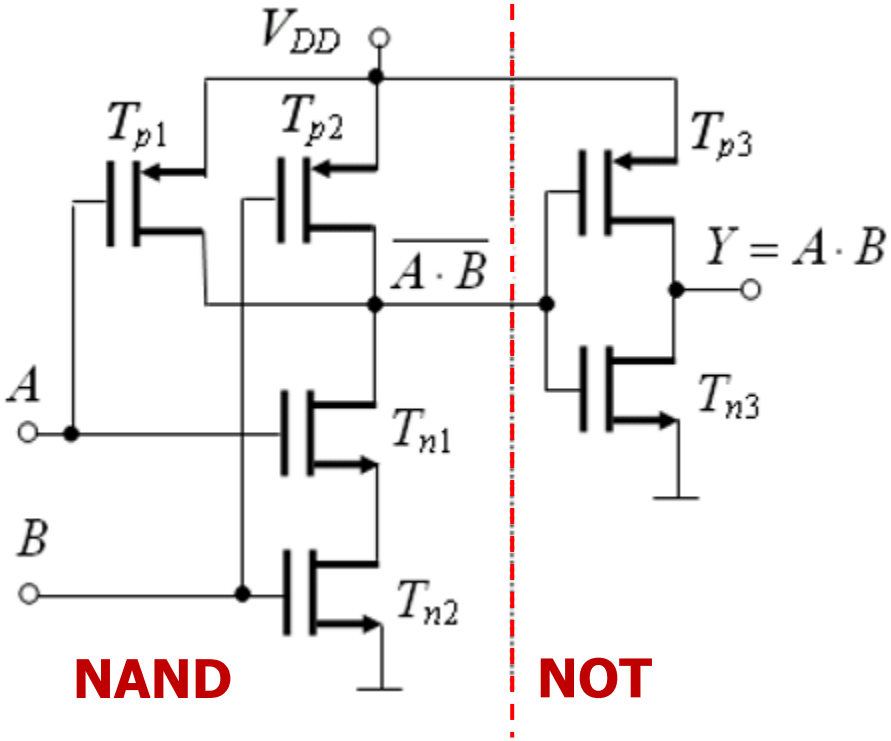




Truth tables?
CMOS logic AND, OR?

Transistor digital circuits

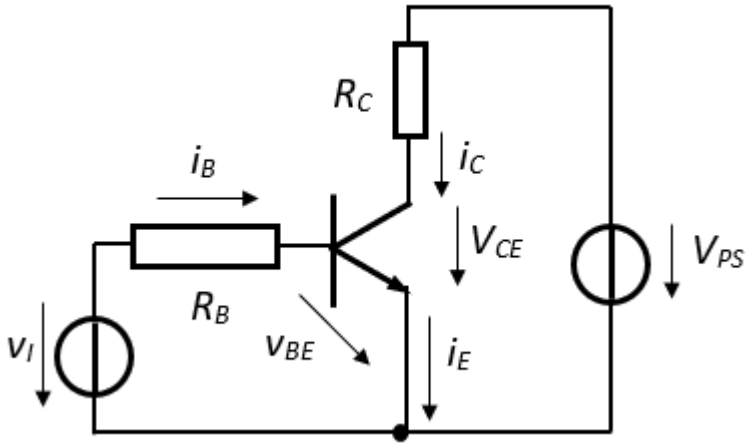
➢ CMOS logic AND

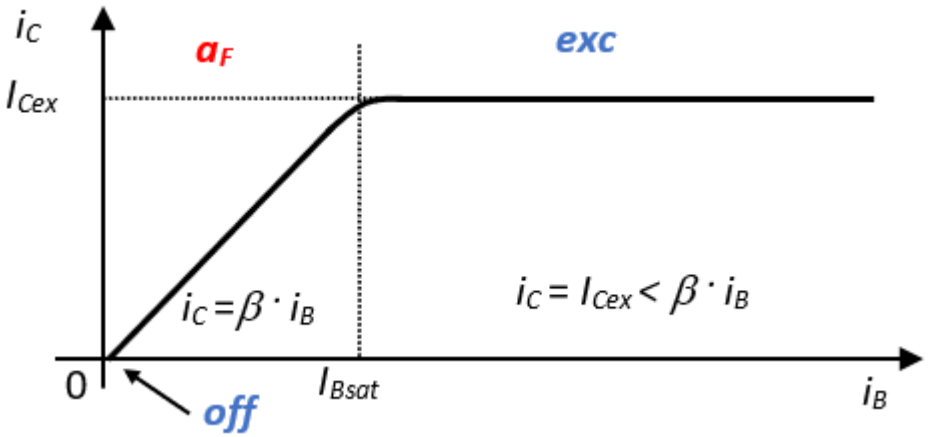


Truth table?
CMOS logic OR?

Transistor digital circuits

➢ BJT digital circuits





$$i_{Cex} = \frac{V_{PS} - v_{CEsat}}{R_C} \approx \frac{v_{PS}}{R_C}$$

$V_{CEsat} \approx 0.2$ V

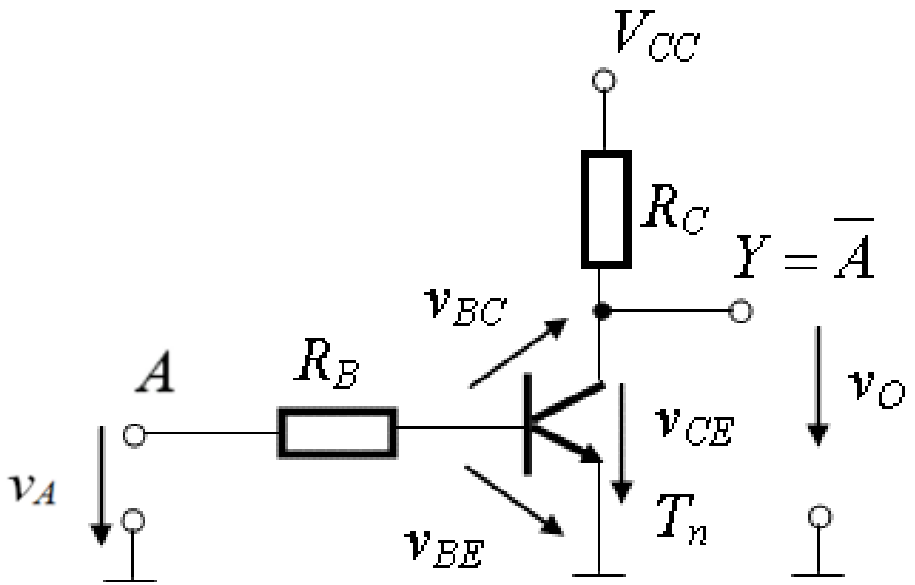
$$i_{Bsat} = \frac{i_{Cex}}{\beta}$$

T – **off**, if $v_I < 0.6$ V

T – **on**, if $i_B > i_{Bsat}$

➢ BJT digital circuits – RTL technology

BJT inverter

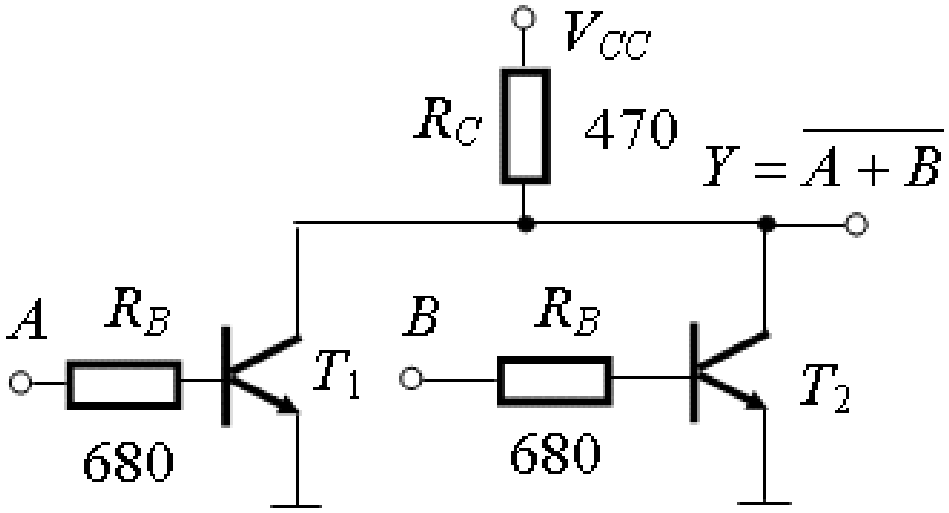


v_A	T_n	v_y
0	off	V_{CC}
V_{CC}	on	$V_{CEsat} \approx 0.2$ V

A	T_n	$Y = \overline{A}$
0	off	1
1	on	0

➢ BJT digital circuits – RTL technology

BJT NOR

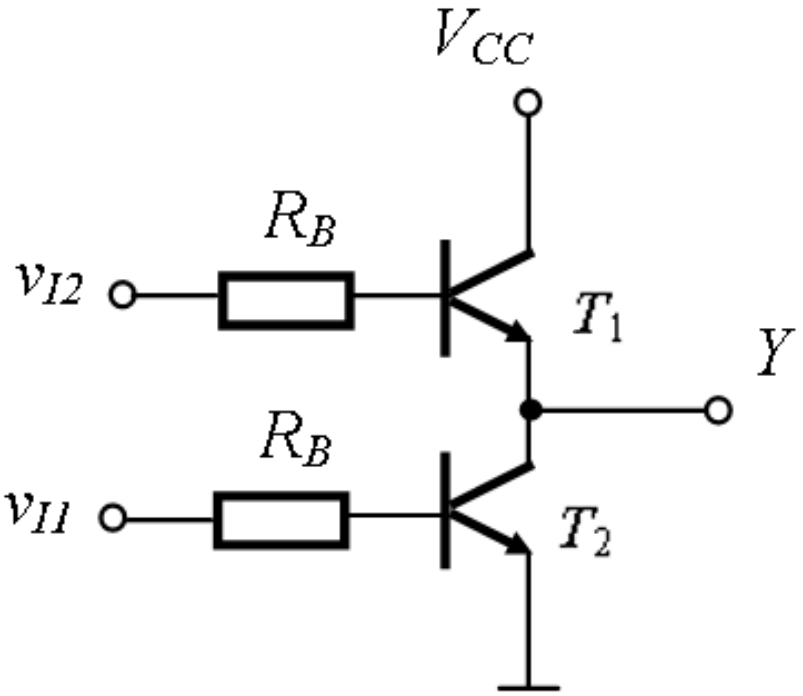


A	B	T_1	T_2	$Y = \overline{A + B}$
0	0	off	off	1
0	1	off	on	1
1	0	on	off	1
1	1	on	on	0

BJT NAND – circuit, truth table?

➢ BJT digital circuits – TTL technology

Logic inverter – npn BJTs; identical transistors, complementary inputs



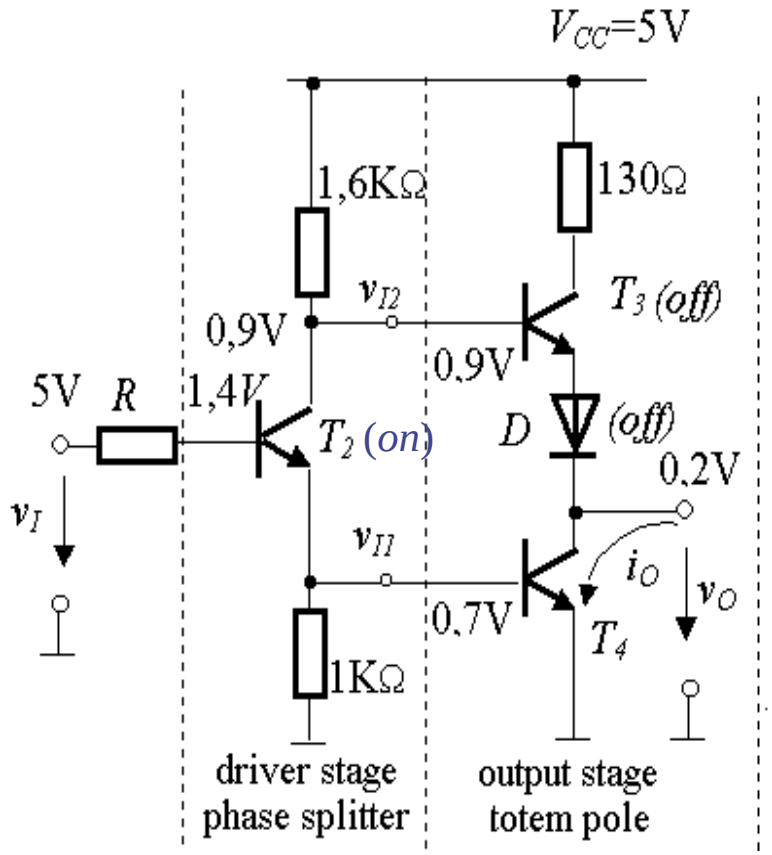
T_1	T_2	Y
on	off	1
off	on	0

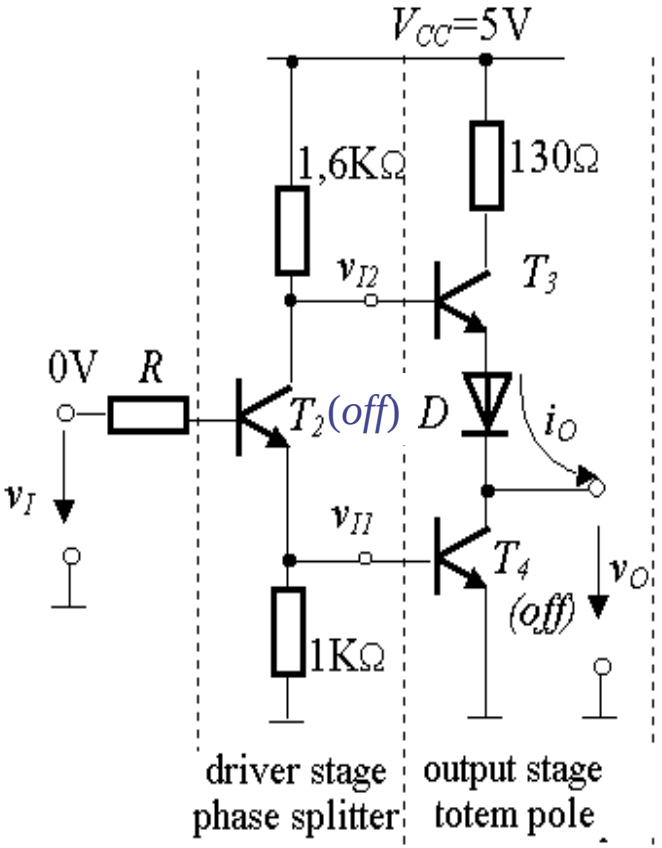
V_{I1}, V_{I2} ?

➢ BJT digital circuits – TTL technology

OPTIONAL

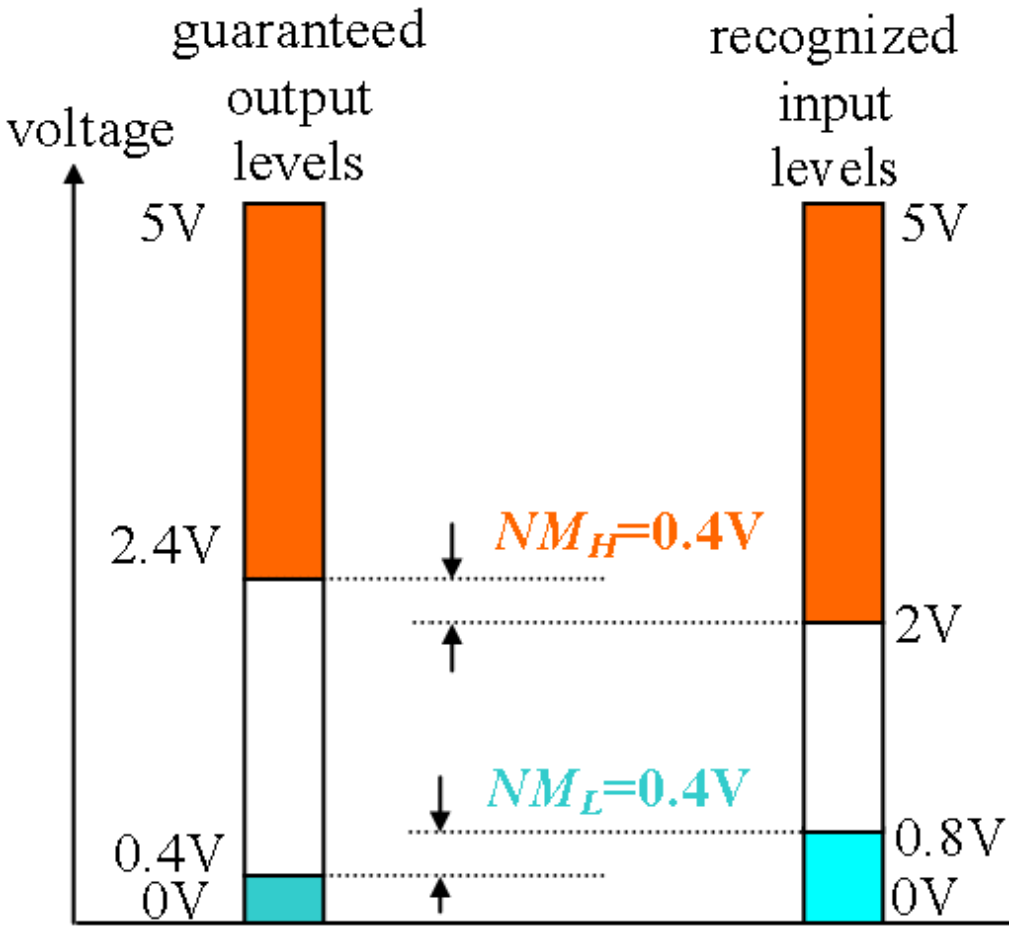
Standard TTL gate





Transistor digital circuits

➢ Noise margins for the TTL logic family, 5 V supply



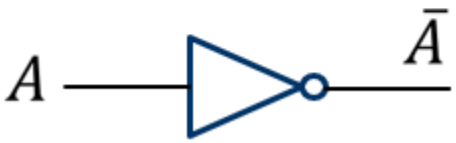
Better/worse than the CMOS family?

Transistor digital circuits

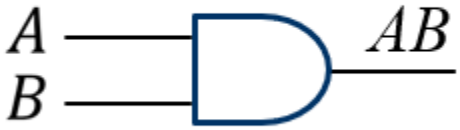
- Logic gates - symbols

OPTIONAL

NOT



AND



OR

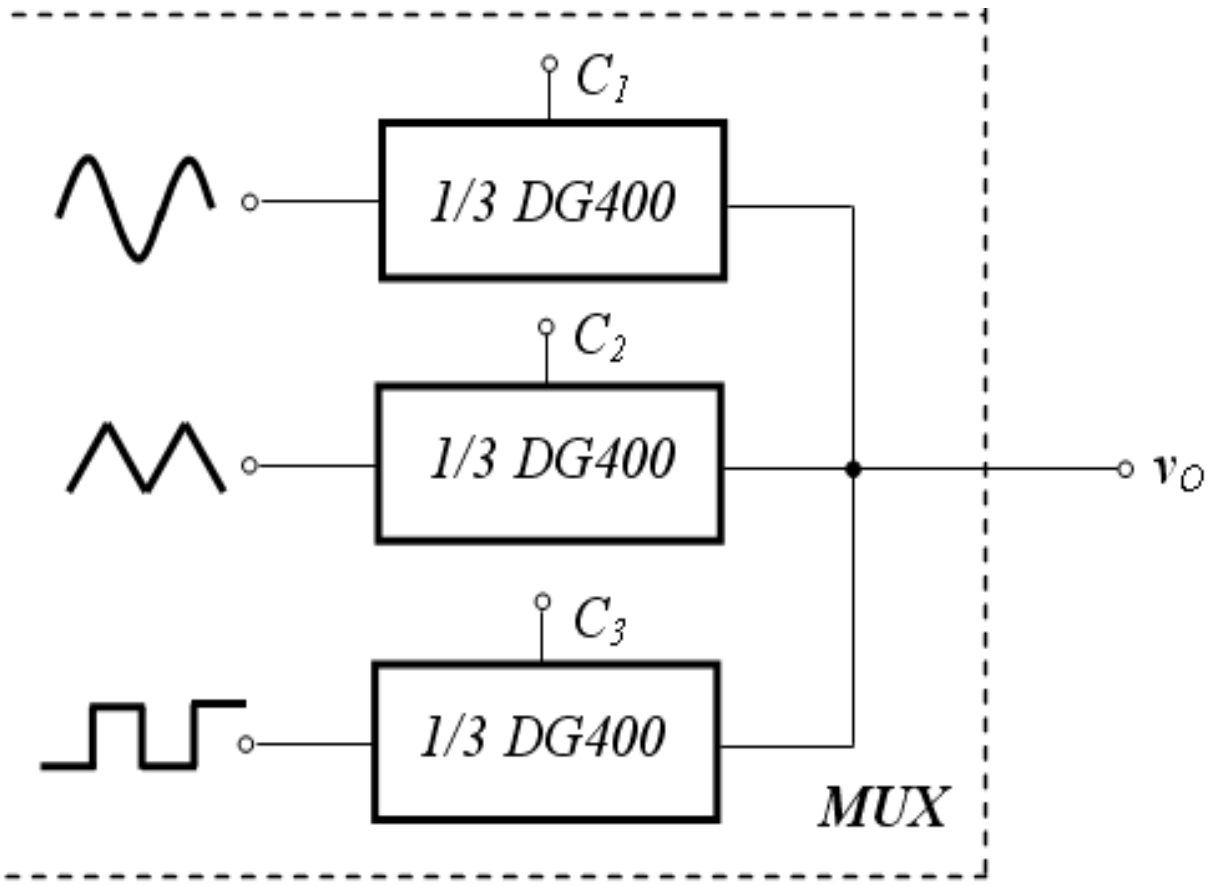
NAND

NOR

XOR

Transistor digital circuits

➢ Application – 3 channel MUX



C_1	C_2	C_3	v_o
1	0	0	∿
0	1	0	⋀⋀
0	0	1	⊓⊓

Summary

- Course presentation
- Evaluation
- Transistors – recap
- Transistor digital circuits

Next week: Transistor amplifiers. DC biasing.