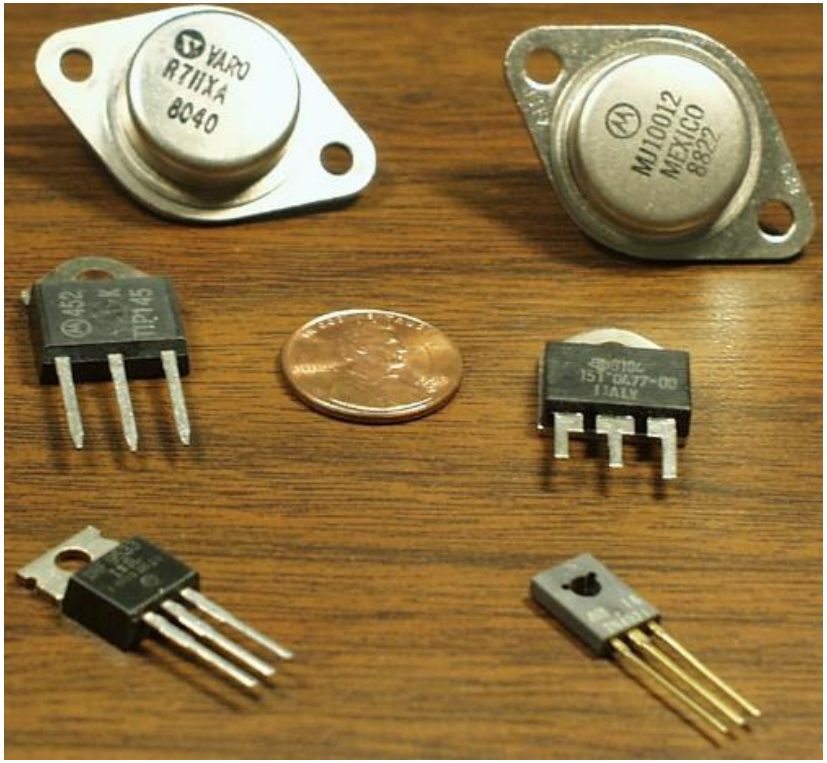
MOSFET Logic Circuits

TRANSISTORS

- **Active** semiconductor devices (with three terminals)
- Operating **principle**: using a **voltage** between two terminals (command) **to control the current** through the third terminal.
- Transistors: ***voltage-controlled current sources***



Discrete transistors

TRANSISTORS

Transistors: essential components of every electronic circuit

Integrated transistors - digital integrated circuit

MOS transistor (T) count (processor)

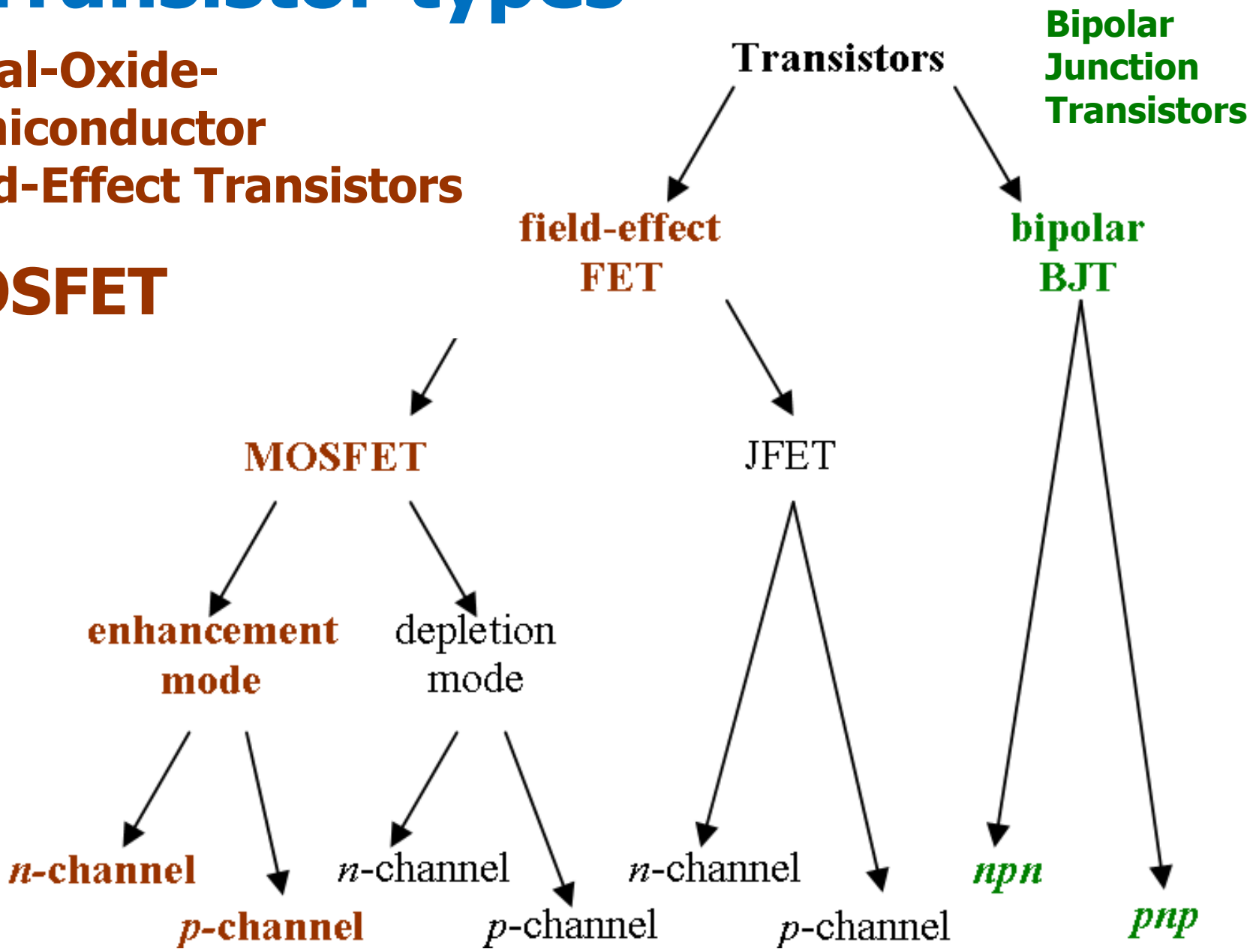
- Intel 4004 (4-bit), 1971, 10µ, 12mm^2, **2,250** T
- Pentium 4 Prescott (32-bit) 2004, 90nm, 110mm^2 **112,000,000** T
- Core i7 Broadwell-E (64-bit), 2016, 14nm, 246mm^2, **3,200,000,000** T
- Apple A12 (hexa-core ARM64), 2018, 7nm, 83.27mm^2, **6,900,000,000** T
- AMD Epyc Rome (64-bit), 2019, 7&12nm, 1088 mm^{2,} **39,540,000,000** T
- Apple M1 Max (10-core, 64-bit), 2021, 5nm, **57,000,000,000** T
- GH100 Hopper GPU, 2022, 4nm, 814mm2, **80,000,000,000 T**

[https://en.wikipedia.org/wiki/Transistor_count]

Transistor types

Metal-Oxide-Semiconductor Field-Effect Transistors

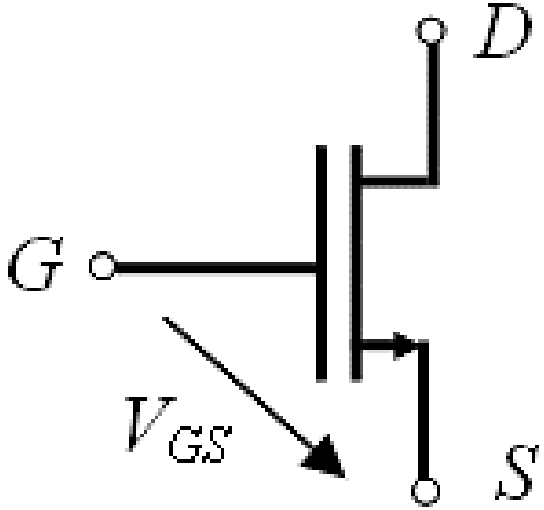
MOSFET



Symbols of MOSFET

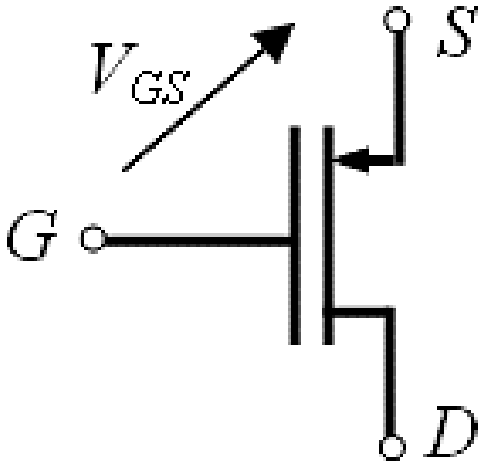
n -channel
enhancement-type
MOSFET

n - type



p -channel
enhancement-type
MOSFET

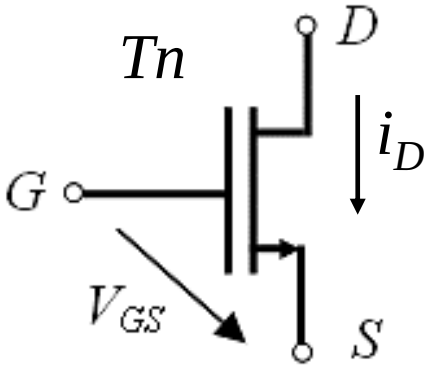
p - type

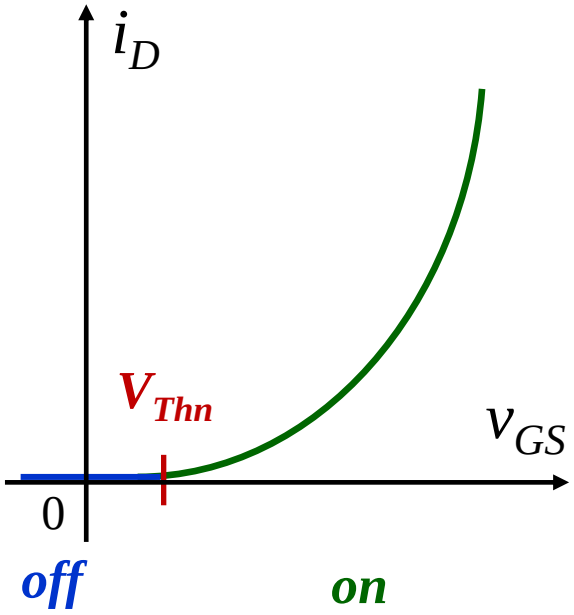


G - gate
D - drain
S - source

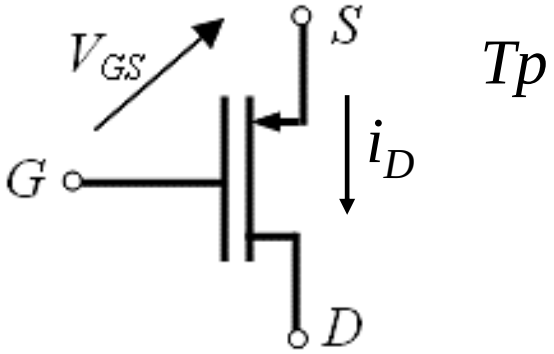
Operation of MOSFET

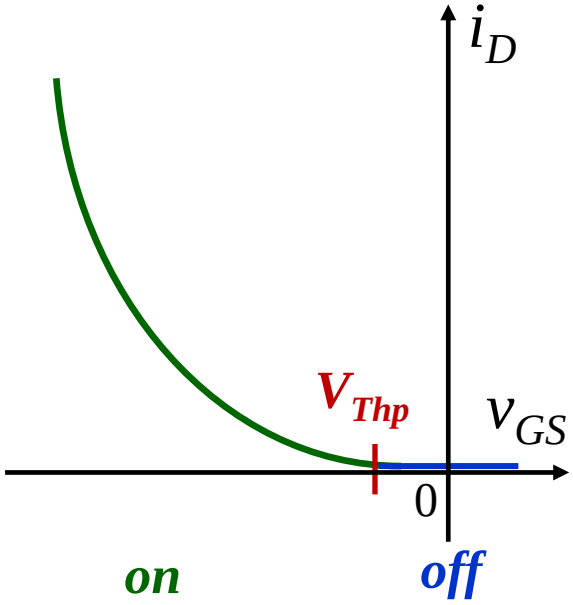
n -channel
enhancement-type **MOSFET**



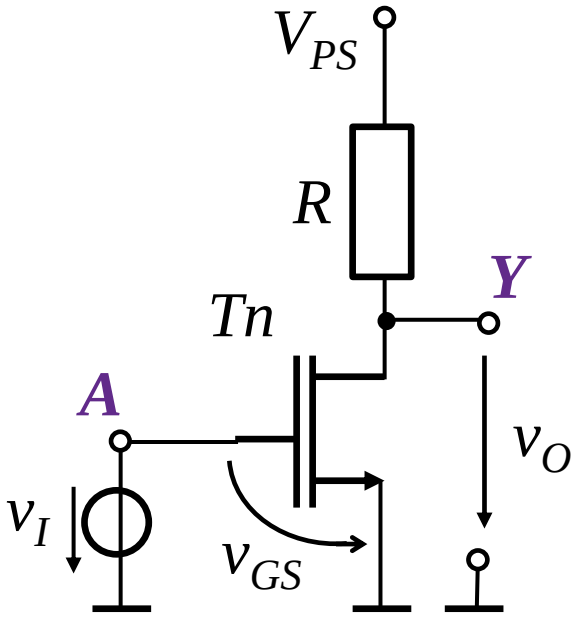


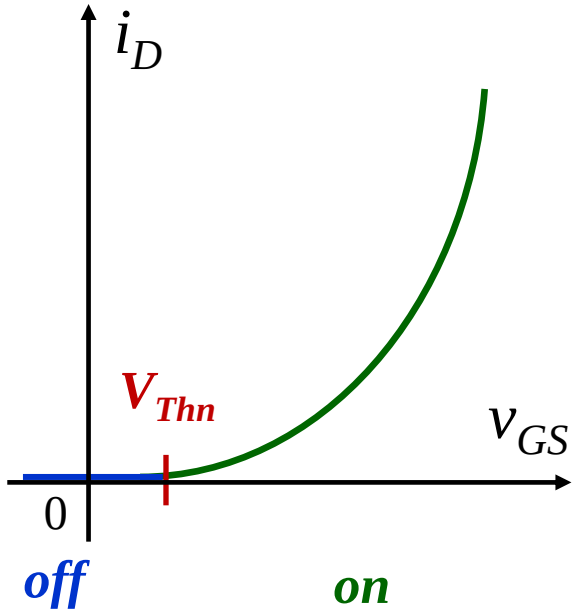
p -channel
enhancement-type **MOSFET**





Logic circuit with *Tn*





0V → logic 0

V_{PS} → logic 1

$$v_{GS} = v_I$$

$$v_I \in \{0, V_{PS}\}$$

Operating table

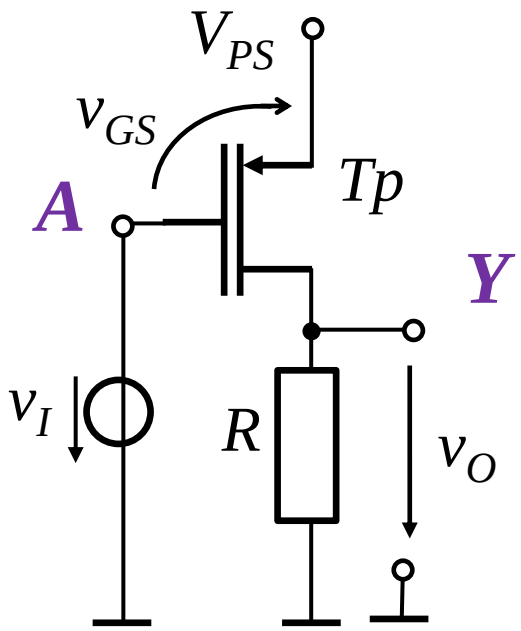
v_I	v_{GS}	*Tn*	v_O
0	0 ($< v_{Thn}$)	*off* (open-circuit)	V_{PS}
V_{PS}	V_{PS} ($>> v_{Thn}$)	*on* (short-circuit)	0

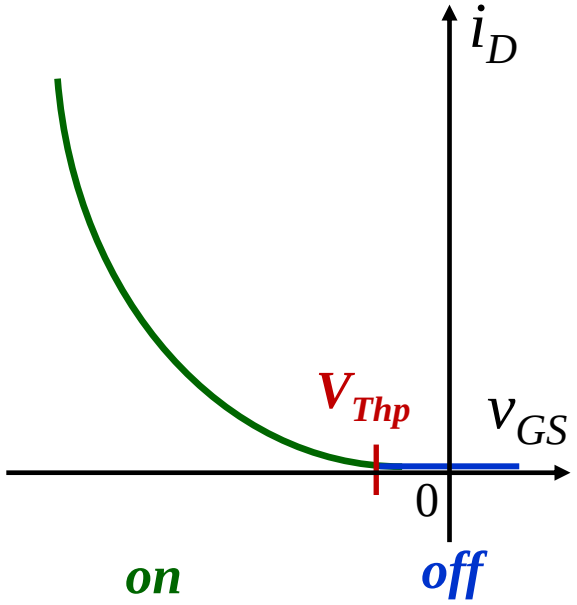
Truth table

A	*Y*
0	1
1	0

NOT

Logic circuit with Tp





0V → logic 0

V_{PS} → logic 1

$$v_{GS} = v_I - V_{PS}$$

$$v_I \in \{0, V_{PS}\}$$

Operating table

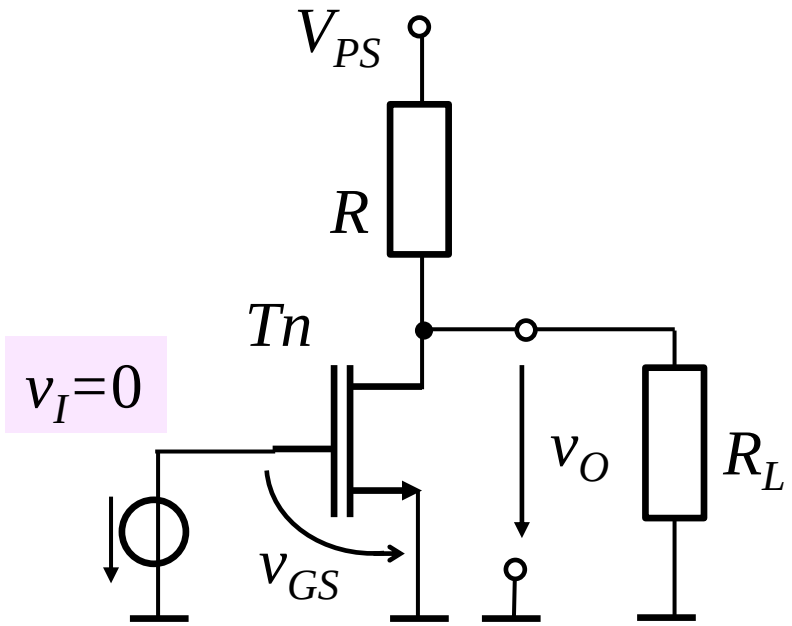
v_I	v_{GS}	Tn	v_O
0	$-V_{PS}$ ($<< v_{Thp}$)	*on* (short-circuit)	V_{PS}
V_{PS}	0 ($> v_{Thn}$)	*off* (open-circuit)	0

Truth table

A	Y
0	1
1	0

NOT

Critical analysis of the NOT logic circuit with T_n and R

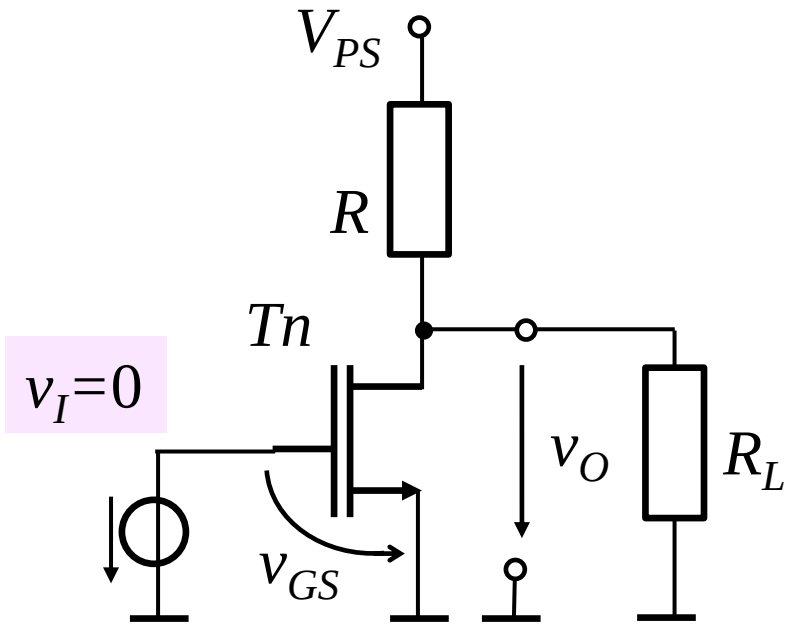


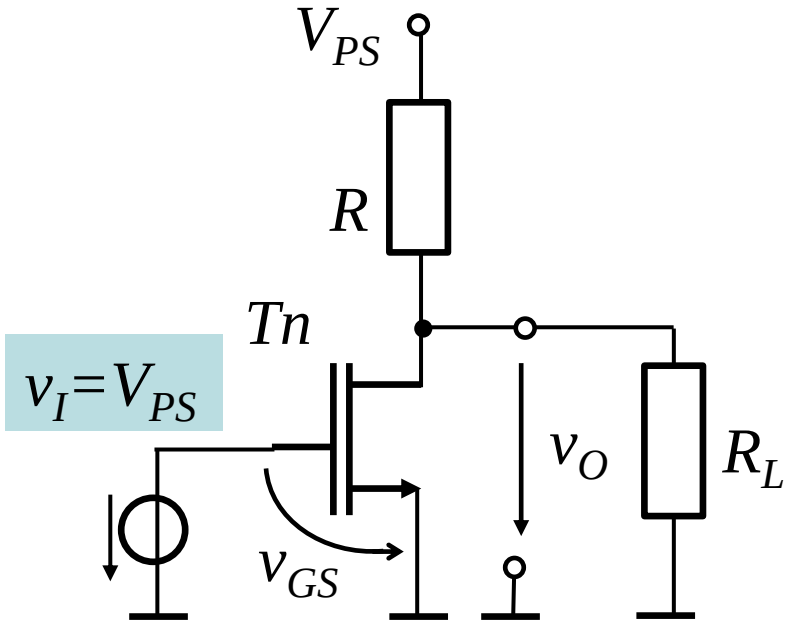
$$v_O = \frac{R_L}{R_L + R} V_{PS}$$

Disadvantage elimination:

***R* as small as possible, ideal *R*→0**

Critical analysis of the NOT logic circuit with T_n and R





$$v_O = \frac{R_L}{R_L + R} V_{PS}$$

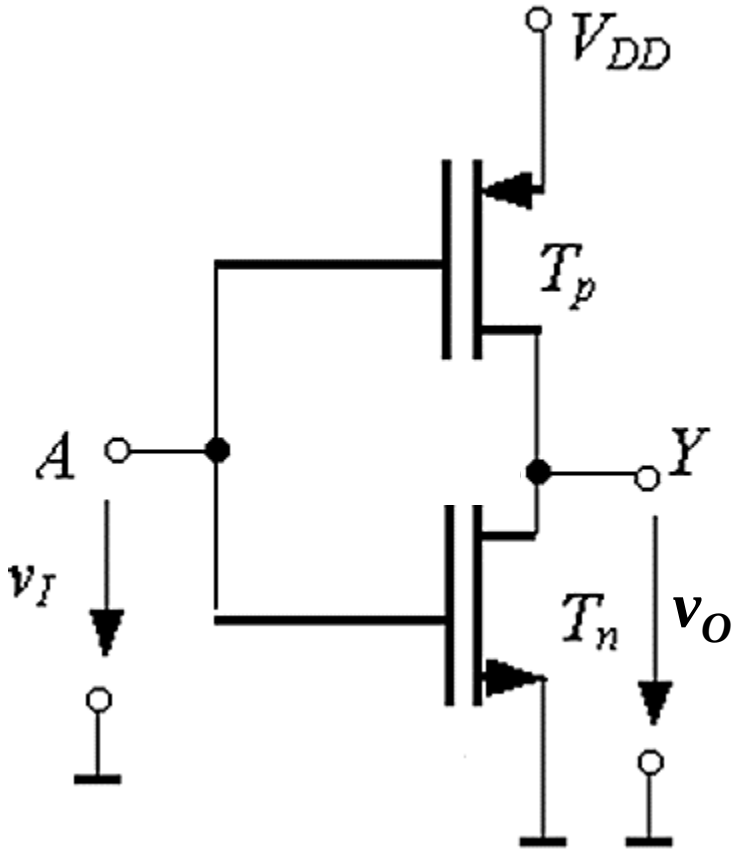
$$P_{PS} = \frac{V_{PS}^2}{R}$$

Disadvantage elimination:

***R* as small as possible, ideal $R \to 0$** ***R* as large as possible, ideal $R \to \infty$**

Solution?

CMOS Logic Inverter

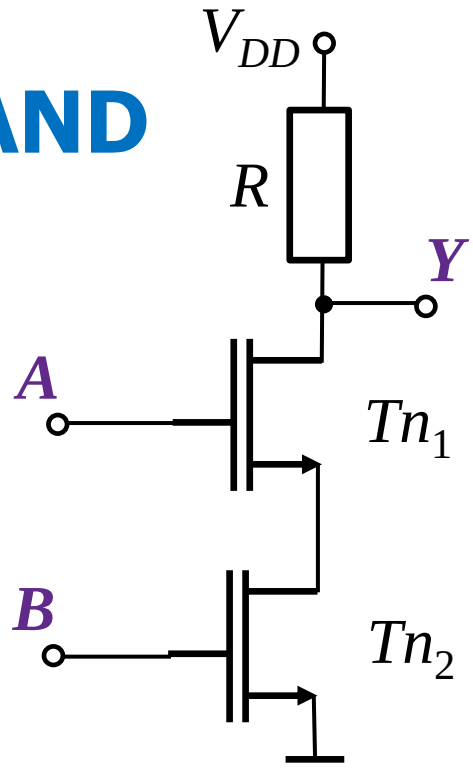


v_I	T_n	T_p	v_O
0V	*(off)*	*(on)*	$\approx V_{DD}$
V_{DD}	*(on)*	*(off)*	$\approx$0V

A	*Y*
0	1
1	0

CMOS – Complementary MOSFET

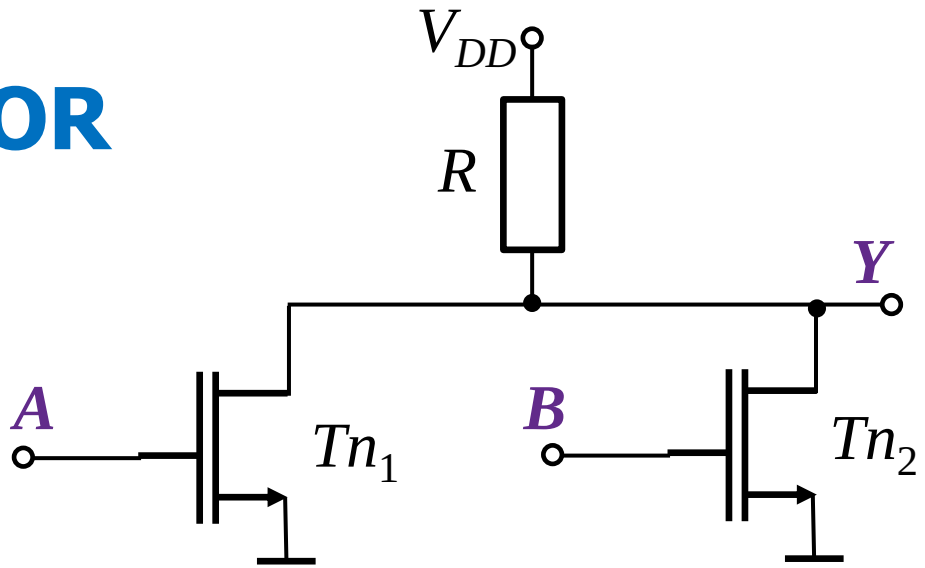
NAND



A	B	T_{n1}	T_{n2}	$Y=\overline{A \cdot B}$
0	0	*(off)*	*(off)*	1
0	1	*(off)*	*(on)*	1
1	0	*(on)*	*(off)*	1
1	1	*(on)*	*(on)*	0

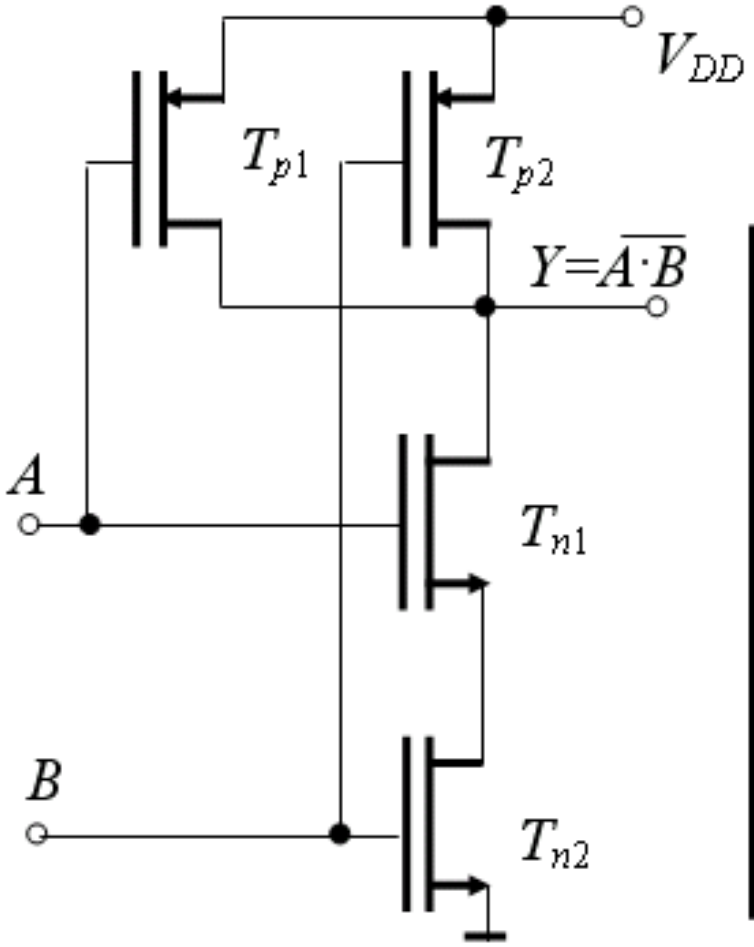
How can we eliminate the disadvantages due to the presence of *R* ?

NOR



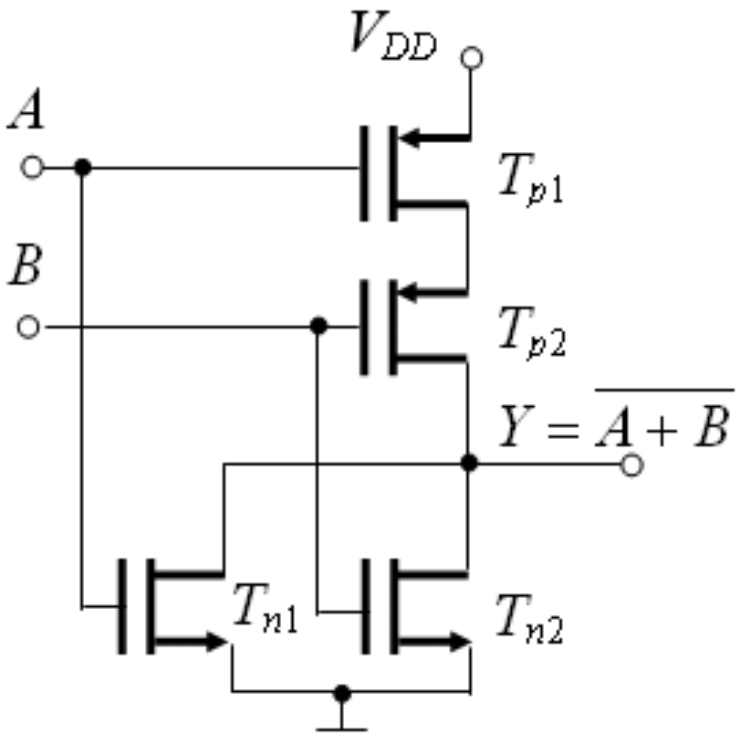
A	B	T_{n1}	T_{n2}	$Y=\overline{A+B}$
0	0	*(off)*	*(off)*	1
0	1	*(off)*	*(on)*	0
1	0	*(on)*	*(off)*	0
1	1	*(on)*	*(on)*	0

CMOS NAND

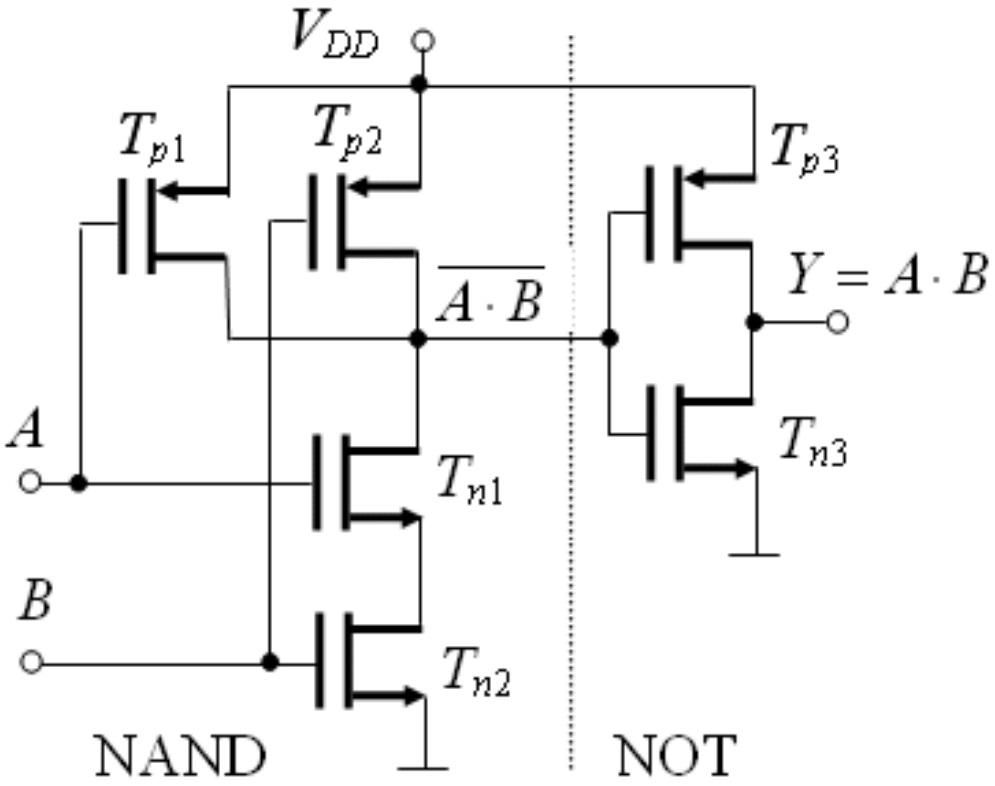


A	B	T_{n1}	T_{n2}	T_{P1}	T_{P2}	$Y=\overline{A\cdot B}$
0	0	*(off)*	*(off)*	*(on)*	*(on)*	1
0	1	*(off)*	*(on)*	*(on)*	*(off)*	1
1	0	*(on)*	*(off)*	*(off)*	*(on)*	1
1	1	*(on)*	*(on)*	*(off)*	*(off)*	0

CMOS NOR

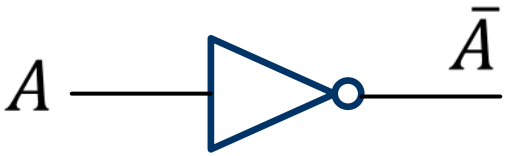


CMOS AND



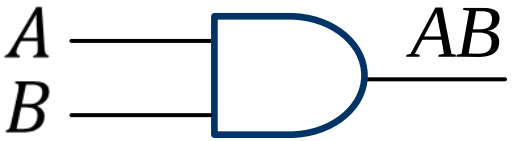
Logic Gates

NOT



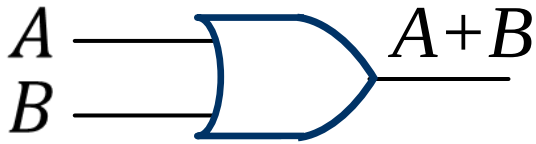
A	$\bar{A}$
0	1
1	0

AND



A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

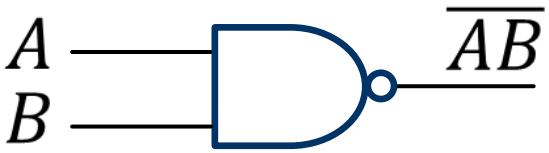
OR



A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	1

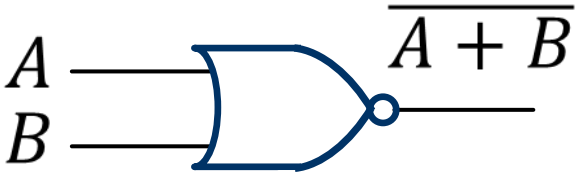
Logic Gates – cont.

NAND



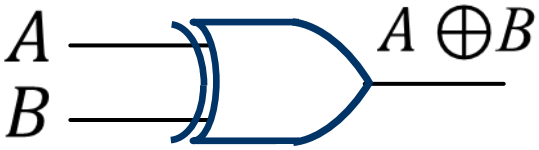
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

XOR



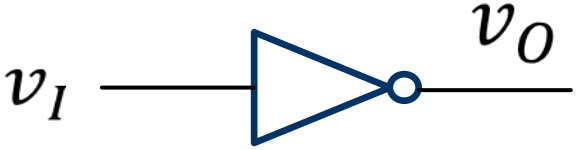
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Problem Use logic gates to implement the logic function:

$$Y = \overline{AB} + A\bar{C}$$

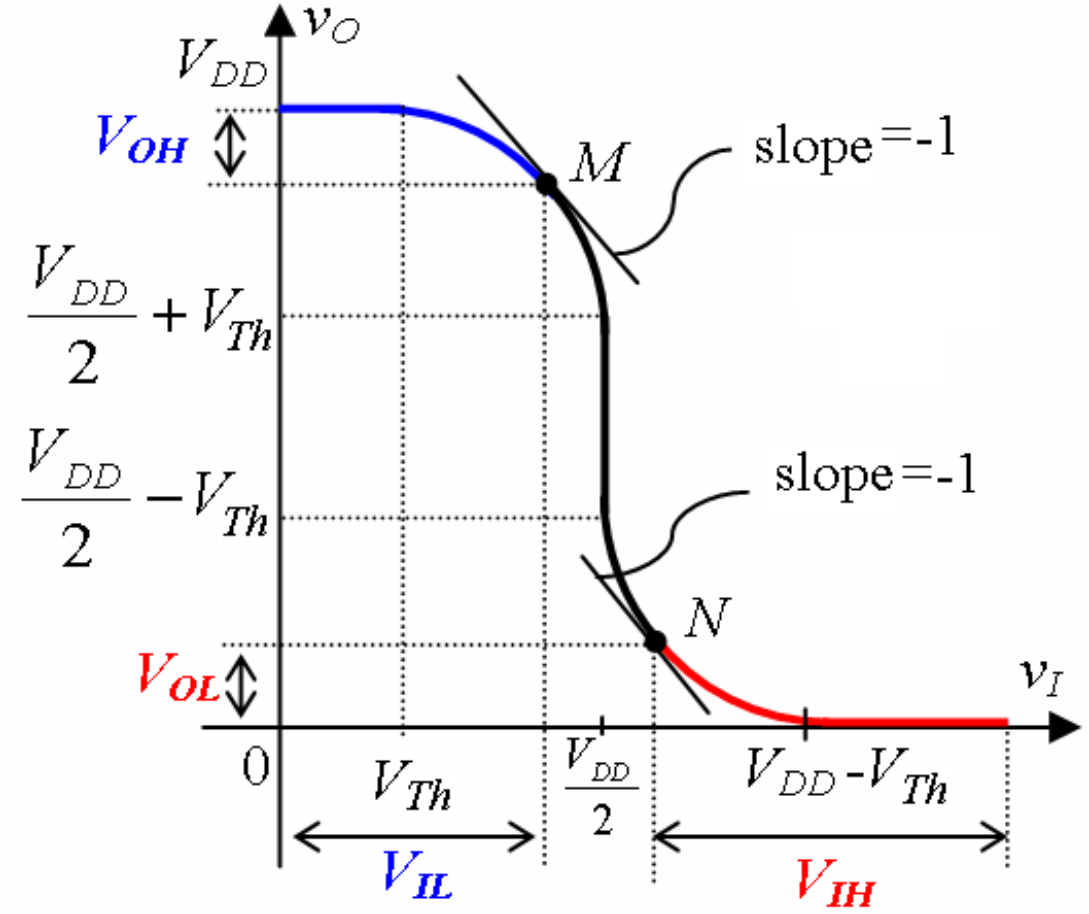
What is the truth table?

Transfer characteristic of the CMOS inverter

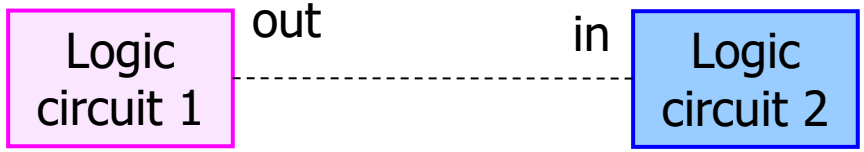


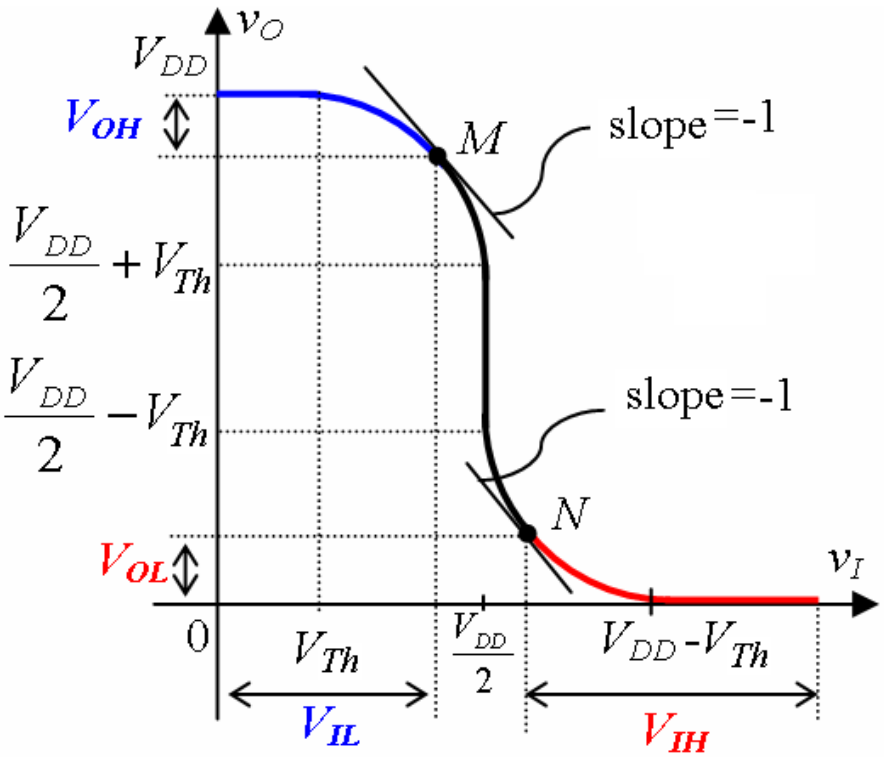
$v_I \in [0;\ V_{DD}]$

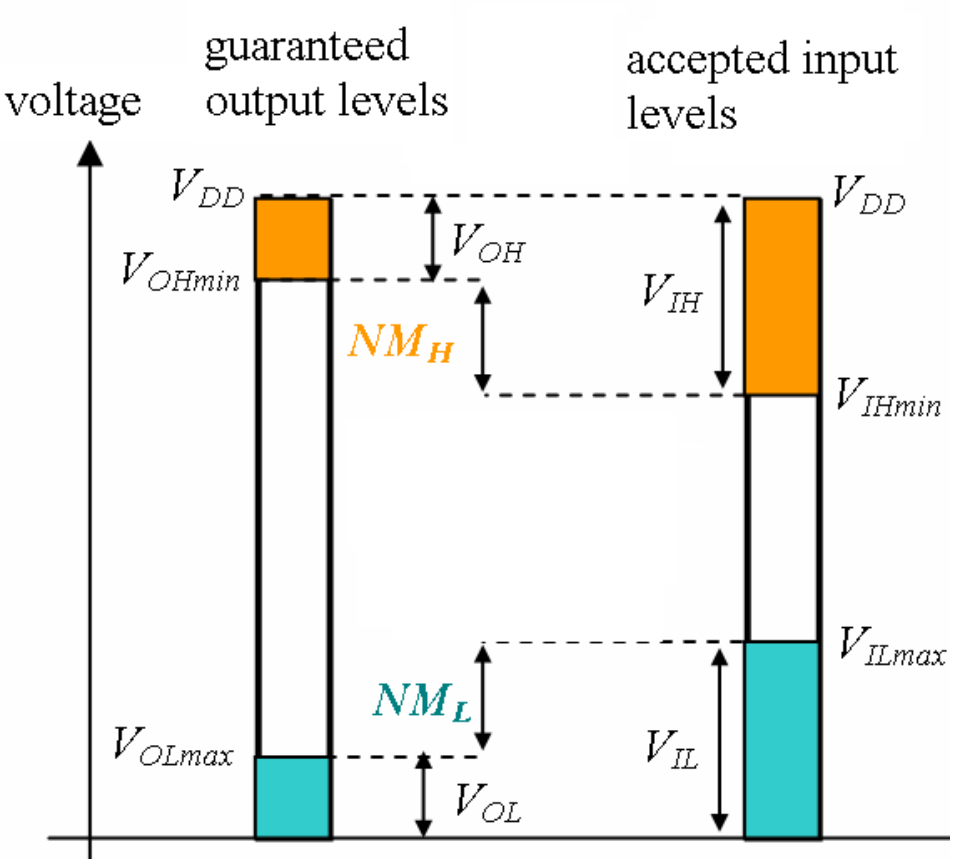
$v_O \in [0;\ V_{DD}]$



Noise margins

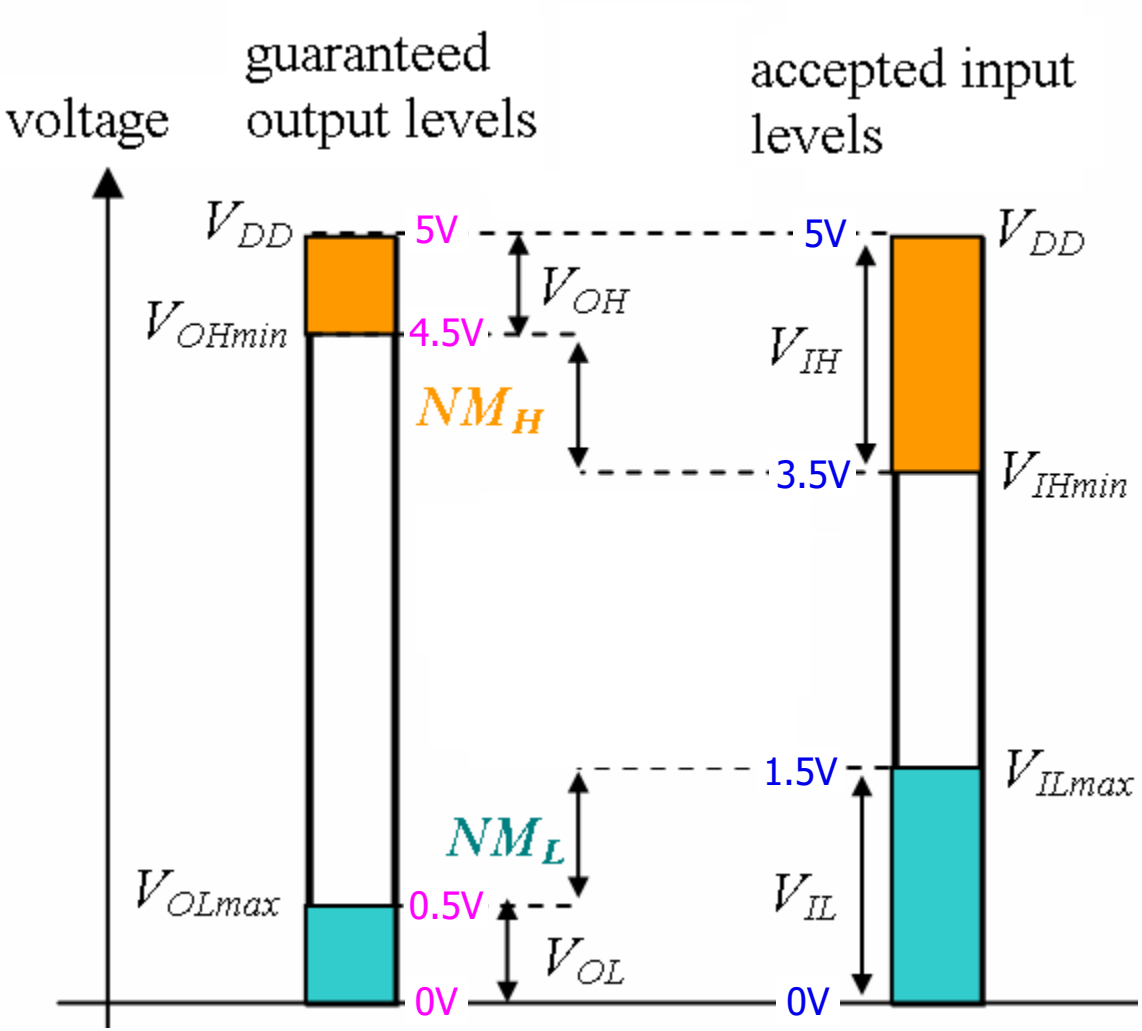






Noise margins - cont.

$$NM_H = V_{OH\min} - V_{IH\min}$$
$$NM_L = V_{IL\max} - V_{OL\max}$$



Voltage levels and noise margins for *CMOS* logic family supplied at +5V

$$NM_L = 1.5\text{V} - 0.5\text{V} = 1\text{V}$$
$$NM_H = 4.5\text{V} - 3.5\text{V} = 1\text{V}$$