LAB 8. MATCHING IMAGE CIRCUITS

8.A. THEORY

The matching image circuits are asymmetric lossless two-ports, with the image impedances of the two-port equal to the equivalent upstream and downstream impedances. Usually the structures in *T* or *Π* are preferred.

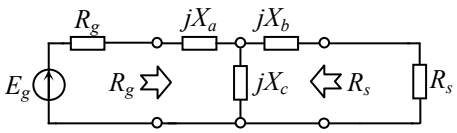

Figure 8.1

Figure 8.1 presents a matching *T*-circuit connected between R_g and R_s. As the arrows suggest, the load R_s is "seen" from the port *1* as a resistance equal to R_g and the resistance R_g is "seen" from the port *2* as a resistance equal to R_s.

The two-port is lossless; therefore the active power is totally transmitted to the load, it results:

$$\left.\begin{aligned} R_g \cdot I_1^2 &= R_s \cdot I_2^2 \\ U_1^2 / R_g &= U_2^2 / R_s \end{aligned}\right\} \Rightarrow \frac{U_1}{U_2} = \frac{I_2}{I_1} = \sqrt{\frac{R_g}{R_s}} = n \qquad (8.1)$$

In other words, the matching circuit behaves likewise a transformer with the ratio *n* (see *(7.3)* from *Lab 7*).

The reactances of the matching *T*-circuit are given by:

$$\begin{cases} X_c = K_{CT} \cdot \sqrt{R_g \cdot R_s} \\ X_a = \pm R_g \sqrt{K_{CT}^2 - 1} - X_c \\ X_b = \pm R_s \sqrt{K_{CT}^2 - 1} - X_c \end{cases} \qquad (8.2)$$

where K_{CT} is a *coupling factor* which can be arbitrarily chosen (positive for *inductive* coupling, or negative for *capacitive* coupling); K_{CT} must satisfies the *coupling condition*: $|K_{CT}| > 1$.

The signs (±) must be the same in both relations: (+) with (+) or (–) with (–). Therefore *4* possible combinations result. All the *4* variants induce the matching, but they behave a little differently, as we'll see further.

As seen in *Lab 7*, the matching circuits – excepting the ideal transformer – induce a phase difference (φ) between the output and the input. In the case of *T*-circuits, φ depends on K_{CT}. Because K_{CT} can be arbitrarily chosen (from the point of view of matching), we can choose a value that induces the wanted φ, according to:

$$K_{CT} = \frac{1}{\sin\varphi} \qquad (8.3)$$

If we denote by α a positive angle $\alpha < \pi/2$, *Table 8.1* shows the *4* possible variants of φ.

Table 8.1

Sign of K_{cT}	*Sign of* $\sqrt{\ }$ *in* X_a, X_b	φ
+	+	α
	–	$\pi-\alpha$
–	+	$-(\pi-\alpha)$
	–	$-\alpha$

From this table, we can make the following remarks:

1) the sign of φ is the same as the sign of K_{CT}:

→ if $K_{CT} < 0$ (*capacitive* coupling) then $\varphi < 0$ (the input leads the output);

→ if $K_{CT} > 0$ (*inductive* coupling) then $\varphi > 0$ (the output leads the input).

2) if $\sqrt{\ }$ and K_{CT} have *the same* sign, then $|\varphi| < \pi/2$; if $\sqrt{\ }$ and K_{CT} have *opposite* sign, then $|\varphi| > \pi/2$.

When we design the matching image circuits, we must also take into account the followings:

1) the frequency characteristics of the matching *T*-circuits are maxim at the work frequency;

2) the two-ports with $\varphi = \pm\alpha$ have a "larger" frequency characteristic, therefore the matching bandwidth is larger, around the work frequency;

3) the two-ports with $\varphi = \pm(\pi - \alpha)$ have a "narrower" frequency characteristic, therefore the matching bandwidth is narrower, around the work frequency.

As a conclusion, if φ is settled then from all *4* variants of two-ports only one variant remains.

8.B. PROBLEMS

8.B.1. If $R_g = 377\Omega, R_s = 188.5\Omega, \alpha = \pi / 6 = 30°$ and the work frequency of *1MHz*, fill in the *Table 8.2* (Δt = is the phase shift (in seconds) between the output and the input.

Table 8.2

Case	φ *[°]*	Δt *[ns]*	K_{cT}	X_c *[Ω]*	*Sign of radical*	X_a *[Ω]*	X_b *[Ω]*
A	*30*				+		
B	*150*				–		
C	*–150*				+		
D	*–30*				–		

8.B.2. With the data from previous problem, fill in the *Table 8.3*, the draw the circuits.

Table 8.3

Case	L_a/C_a	L_b/C_b	L_c/C_c
A			
B			
C			
D			

8.C. LAB WORK

Using the data from case *A* (*Table 8.3*), draw in *OrCAD* the circuits from *Figure 8.2*.

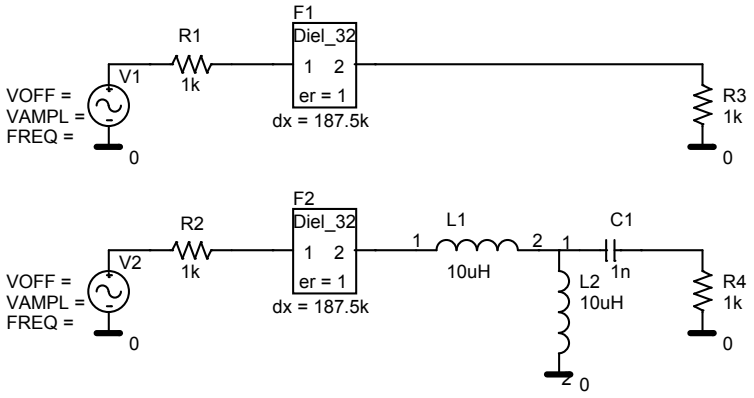

Figure 8.2

Set the following parameters:

→ the sources: offset *0V*, amplitude *1V*, frequency *1MHz*, *AC = 1V*;
→ the resistances of the sources: *377 Ω*; the load resistances: *188.5 Ω* (half of the source's resistance);
→ the parts *DIEL_32*: *dx = 9.375* ;
→ *La*, *Cb* and *Lc* with the values from *Table 8.3*.

8.C.1. First create all the profiles that you'll need in this lab:

1) **a time profile** with the name *"timeA"* of *Time Domain* type (*Run to time = 10μs*, *Maximum Step Size = 4ns* and check the *SKIPBP* checkbox). Then create another *3* identical profiles, named *"timeB"*, *"timeC"* and *"timeD"* (use *Inherit From*).

2) **a frequency profile** with the name *"freqA"* of *ACSweep/Noise* type (between *100kHz* and *10megHz*, *100* points / decade). Then create again another *3* identical profiles, named *"freqB"*, *"freqC"* and *"freqD"*.

Make active the "*timeA"* profile and run the simulation. Make active the "*freqA"* profile and run the simulation. Then for each from the cases *B*, *C* and *D*, follow the steps:

1) go back to the schematics and modify the matching circuit of the case, using the data from *Table 8.2*;
2) make active the time profile of the case and run the simulation;

3) make active the frequency profile of the case and run the simulation;
4) repeat from step *1)* for the next case.

After each running, *OrCAD* has created a "*.dat*" file, so in this moment there are *8* "*.dat*" files, corresponding to the *8* runnings. In the rest of the lab you don't have to run anymore, just open the "*.dat*" file that you need.

8.C.2. First we'll study **the time behavior**. Close all the windows in frequency and let open all the windows in time. In each window, do the followings:

- add a new plot;
- display with **ADD TRACE** the following *4* voltages:
  - → in the upper plot: from the *1st* circuit: *(1)* the input voltage of the delay line and *(2)* the difference between this voltage and the voltage that would be in case of matching (half of the source's voltage); this difference represents the reflected wave;
  - → in the lower plot: from the *matched* circuit: the same two voltages as above.

In any window, compare the two plots and notice:

- in the *1st* circuit: the reflected wave appears after $2\mu s$ (which is the necessary time to propagate through the delay-time and back); the effect is the decreasing of the amplitude.
- in the *matched* circuit: after $2\mu s$ a transitory sate begins, then the amplitude comes back to the value that correspond in matching. The conclusion is that the matching is realized after the transitory state ends.

In the other windows, observe that the shape and the duration of transitory state differ depending on the case.

8.C.3. Close the *4* windows and re-open two times the *"timeA.dat"* file (with the button **OPEN**). Now we'll study the waves in the **matched** circuit.

In the first window, display the input voltage of the delay line. Add another *Y*-axis (*Plot → Add Y Axis*), and display here the current through *Rg* (which is also the current through the equivalent input impedance of the delay line). Measure the voltage amplitude (U_1) and the current amplitude (I_1) at the input of the delay line (after the transitory state, so after $5\mu s$) and fill in the *Table 8.4*.

In the second window, display the voltage and the current through the load (for the current use another *Y*-axis, as before). Measure the voltage amplitude and the current amplitude (U_2 and I_2), (after the transitory state) and fill in the *Table 8.4*.

Table 8.4

U_1	I_1	U_2	I_2	Z_1	P_1	P_2

Compute the input impedance of the delay line (Z_1) and compare it with the source resistance (377Ω). A perfect matching means that the two are equal.

Compute the active powers in the input section of the delay line (P_1) and on the load (P_2) and fill in. Theoretically, these powers should be equal. The small difference between them – the same as the difference regarding the input impedance in the delay line – are due to the imperfections of the models, inclusive the transitory state which, theoretically, is infinite. The errors decrease if "*Run to time*" from the profile is increased.

8.C.4. Close the two windows and open, again, all the 4 time files: *"timeA"*, *"timeB"*, *"timeC"* and *"timeD"*.

In each window, display the input voltage of the matched circuit and the voltage on the load. Measure the phase difference between the output and the input (Δt).

Take the values of Δt *computed* from *Table 8.2*. Compute also φ and the errors (in %) and fill in the *Table 8.5*.

Table 8.5

Case	Δt			φ		
	computed	*measured*	*error*	*computed*	*measured*	*error*
A				*30*		
B				*150*		
C				*-150*		
D				*-30*		

8.C.5. Now we'll study **the frequency behavior** of the matching circuits.

Close the windows *"time"* and open the *4 "freq"* files. In each window, display the voltage on the load.

Because for each source *AC* is *1V*, the load voltage vs. frequency is actually the gain characteristic.

Observe the selective frequency behavior of each matching circuit. Measure the maxims of the gains and the frequency that they are at.

Also notice:

- the matching circuits with $|\varphi| < \pi / 2$ have larger" frequency characteristics, therefore the matching bandwidth is larger, around the work frequency.
- the matching circuits with inductive coupling (transverse inductance) have an inclination to *HPF* characteristic, and the matching circuits with inductive coupling – to *LPF* characteristic.

NOTE: The oscillations of the characteristics at high frequencies are due to the delay line model. As proof of this, remove the delay lines from the schematics and repeat the frequency analyses. You'll see that the characteristics will be smooth.